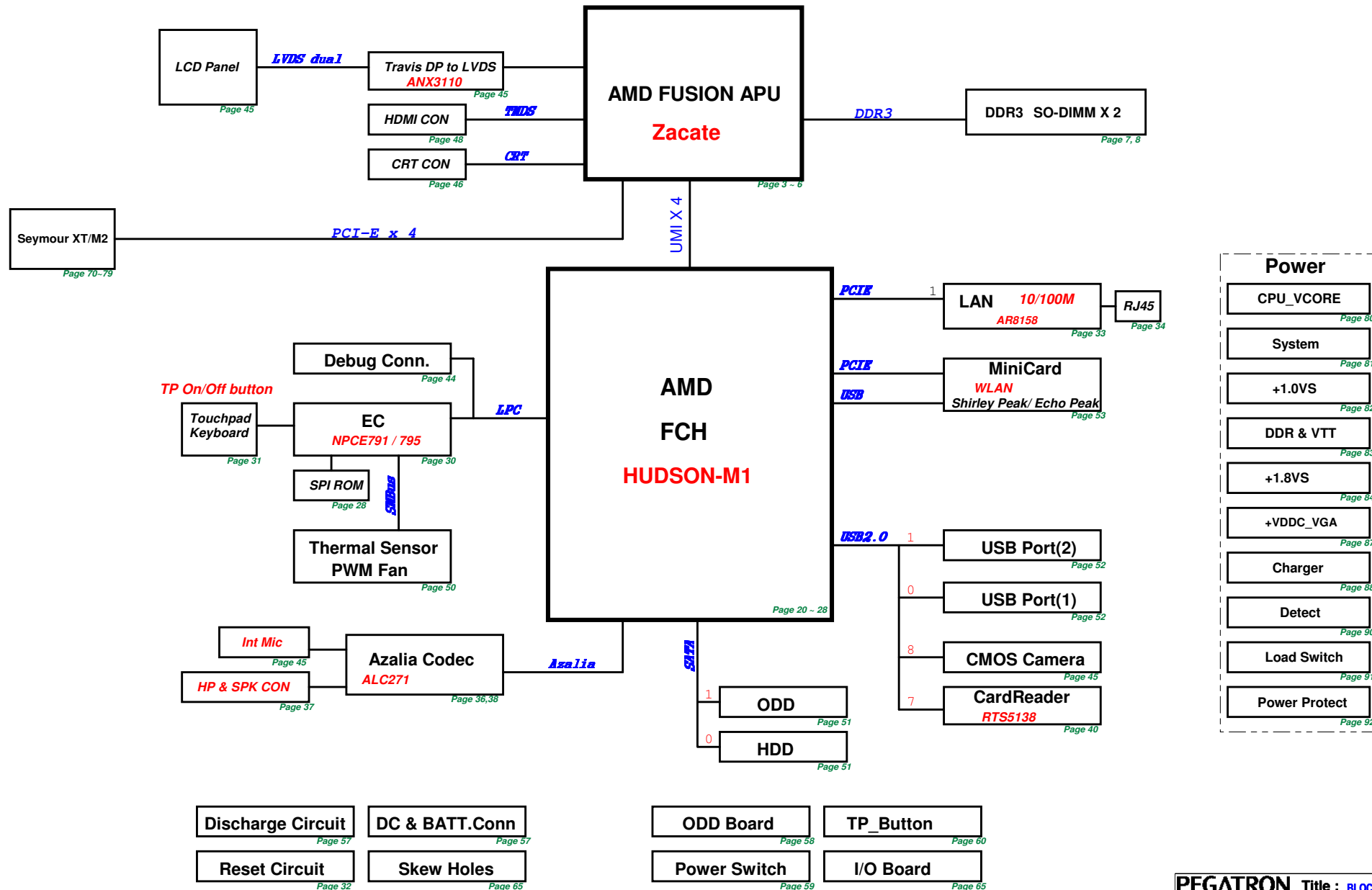


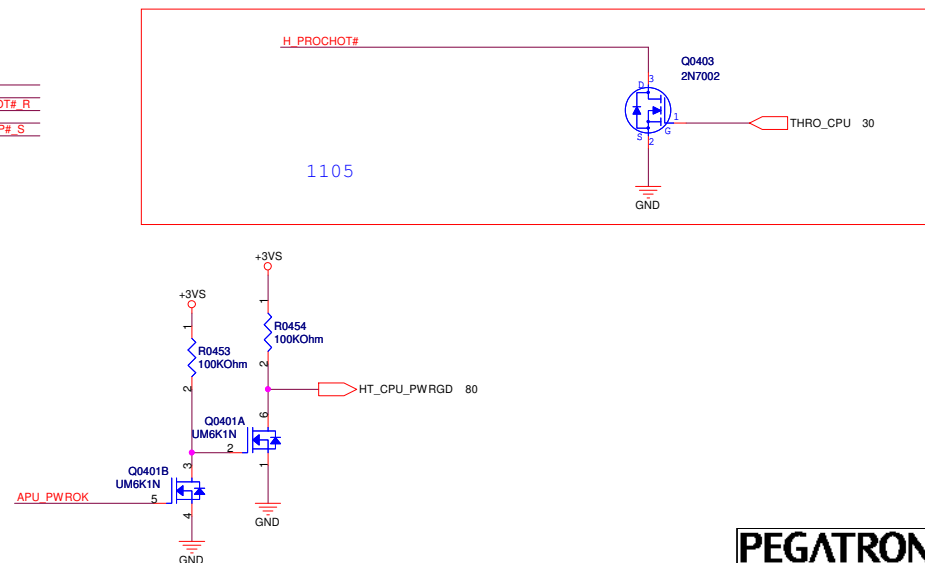
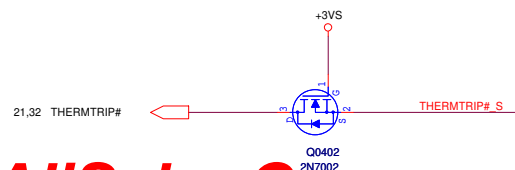
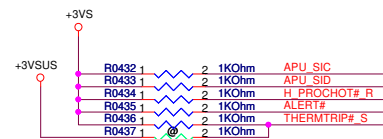
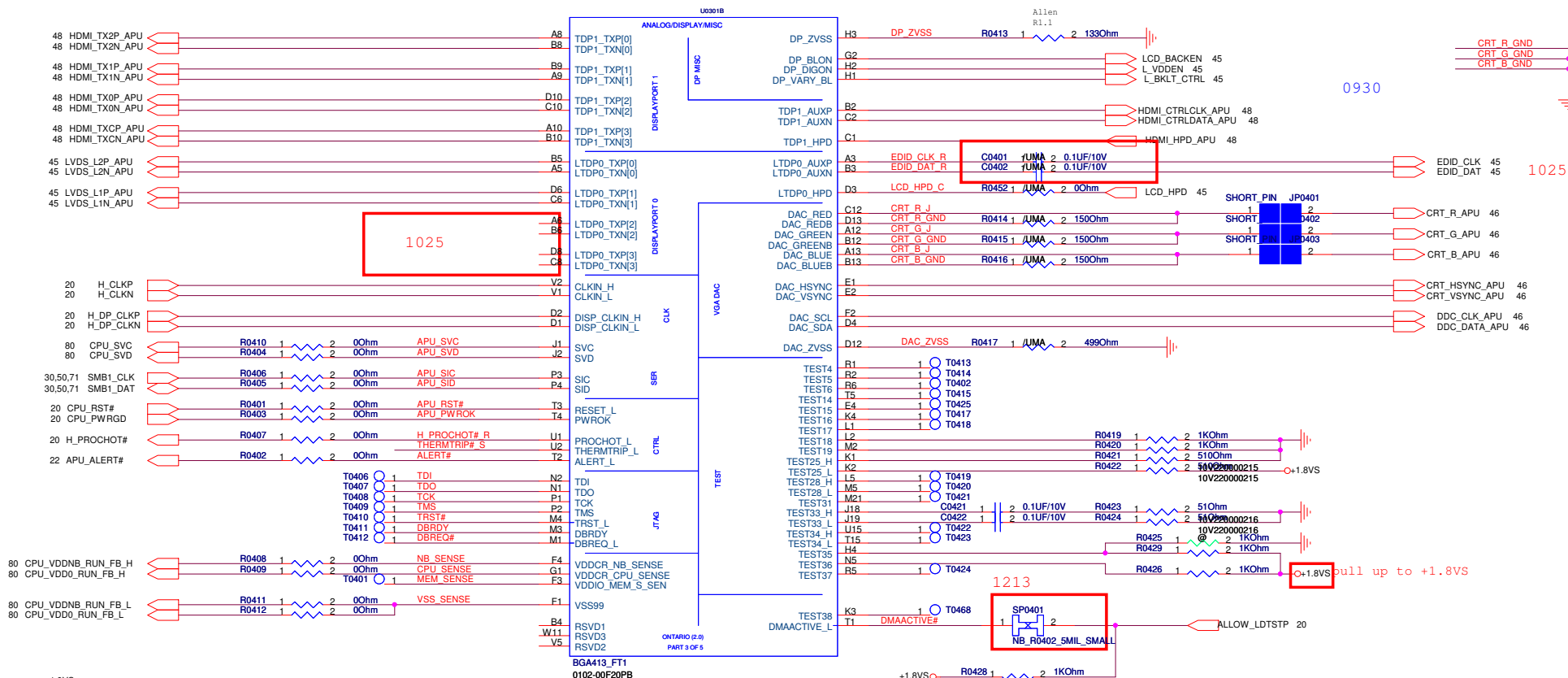
AAB70 AMD Brazos Platform Rev. 2.0

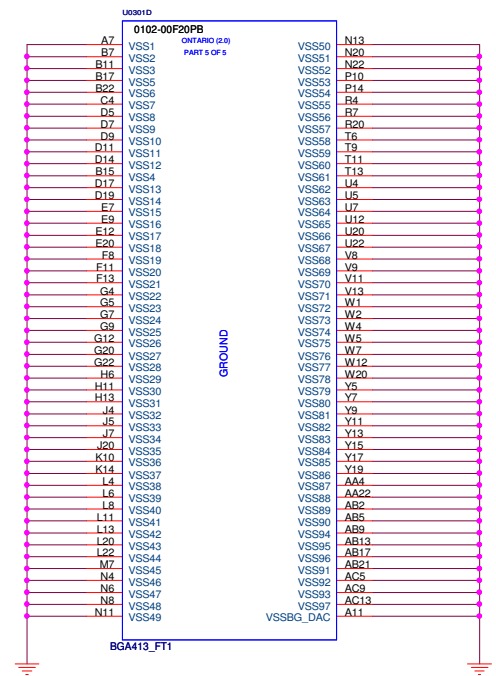
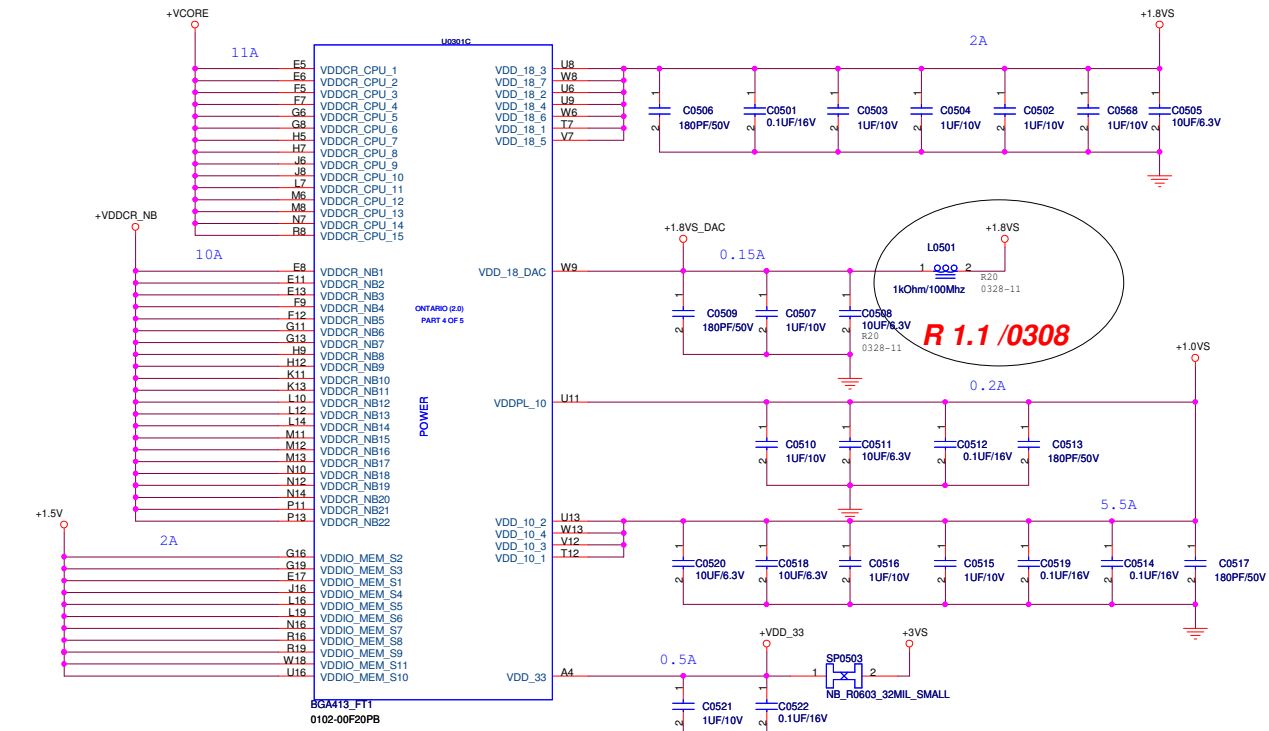
BLOCK DIAGRAM

R 1.1 /0301



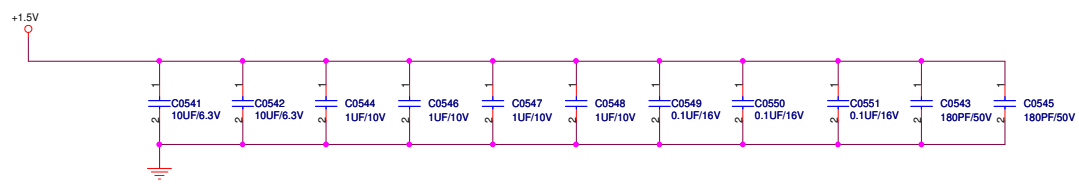
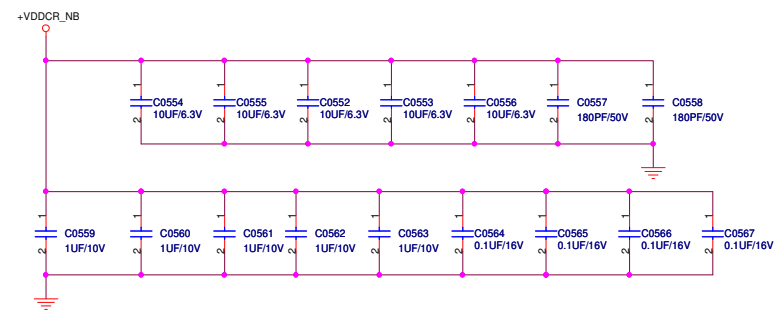
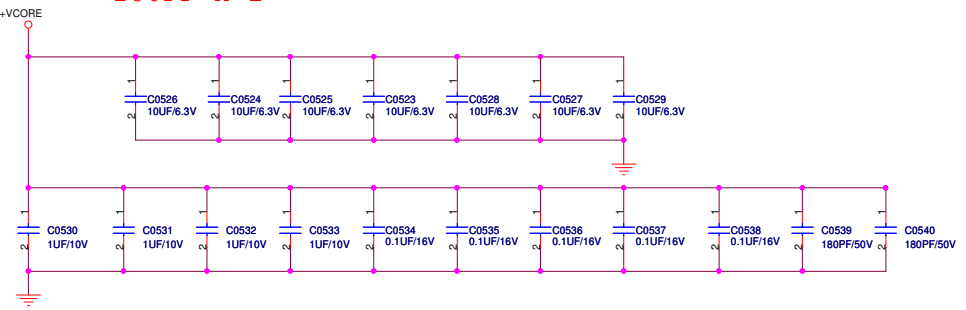






+VCORE
 10UF x 7
 1UF x 4
 0.1UF x 5
 180PF x 2

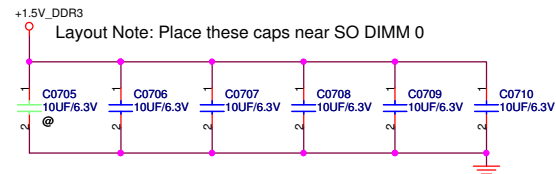
+VDDCR_NB
 10UF x 7
 1UF x 4
 0.1UF x 5
 180PF x 2





PEGATRON		Title : CPU(4)_PWR	
		Engineer: Allen_CD_Wu	
Size	Project Name		Rev
Custom	AAB70		1.1
Date: Monday, March 21, 2011		Sheet	6 of 99

1202-002H000

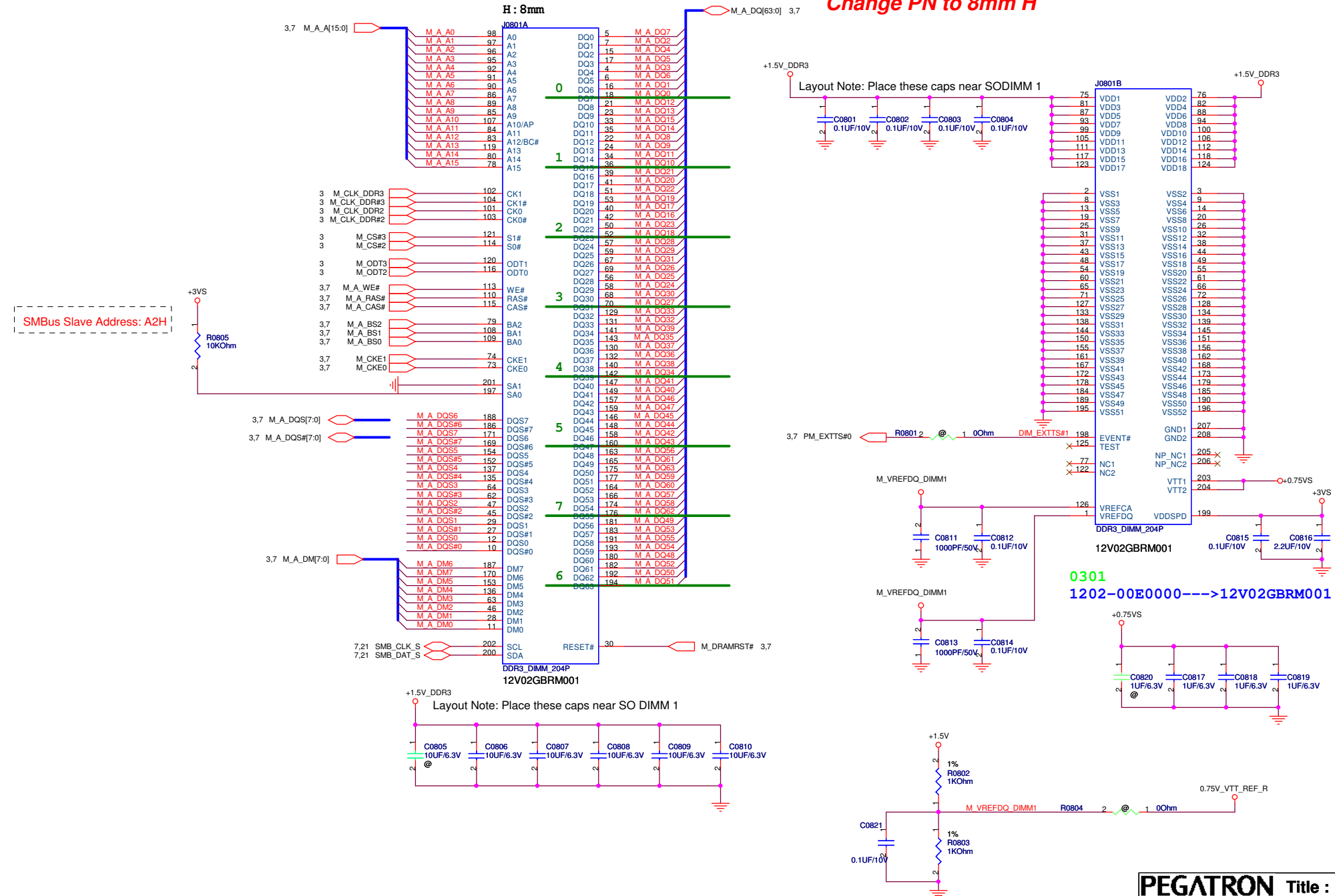


Date: Thursday, April 21, 2011 Sheet 7 of 99

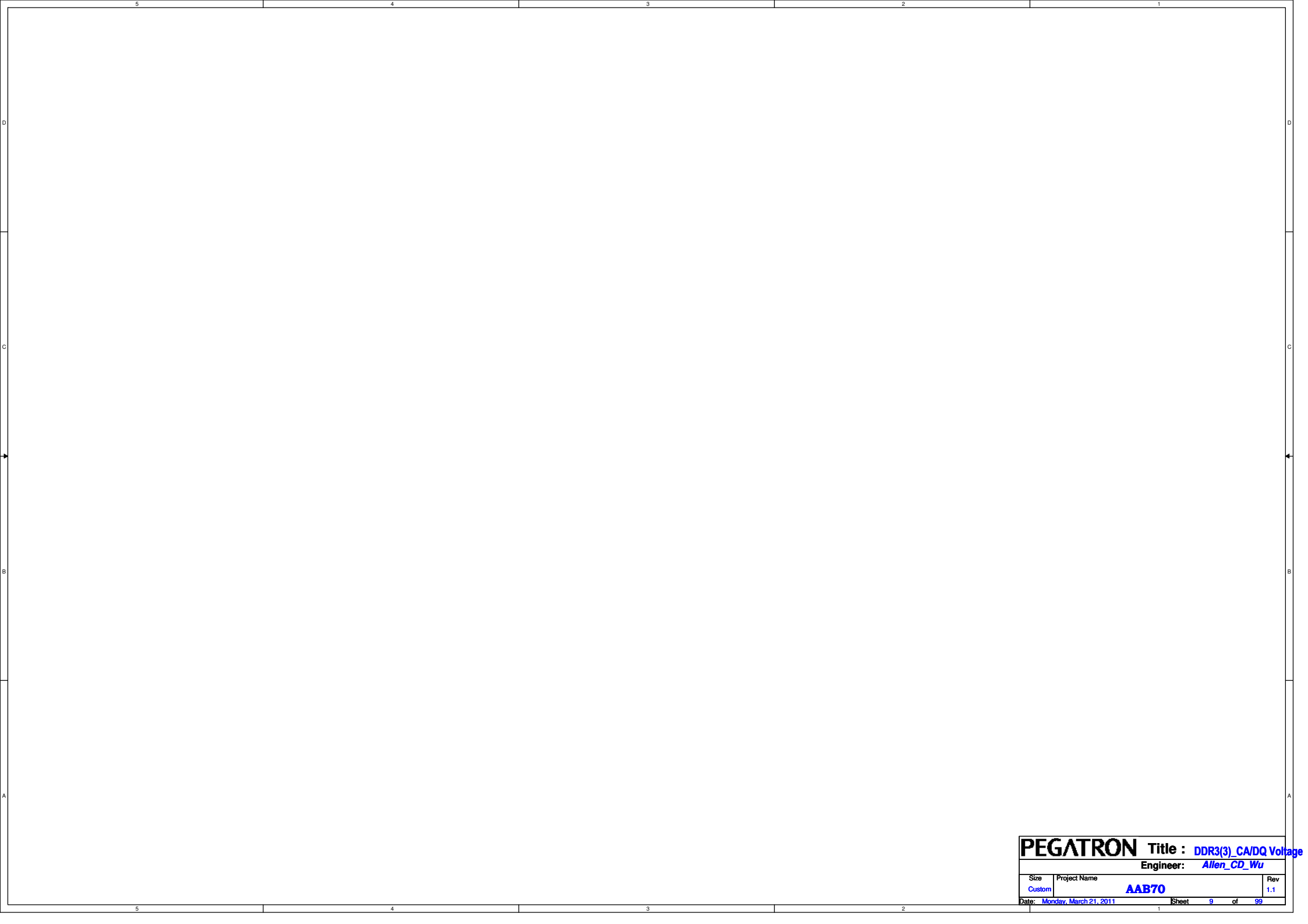
1202-000P000

R 1.1 /0308

Change PN to 8mm H



PEGATRON				Title : DDR3(2)_SO-DIMM1	
				Engineer: Allen_CD_Wu	
Size	Project Name				Rev
Custom	AAB70				1.1
Date: Thursday, April 21, 2011			Sheet 8 of 99		



PEGATRON		Title : DDR3(3)_CA/DQ Voltage	
		Engineer: Allen_CD_Wu	
Size	Project Name		Rev
Custom	AAB70		1.1
Date: Monday, March 21, 2011		Sheet	9 of 99

1014

0929

1213

1213

1213

0930

0929

1213

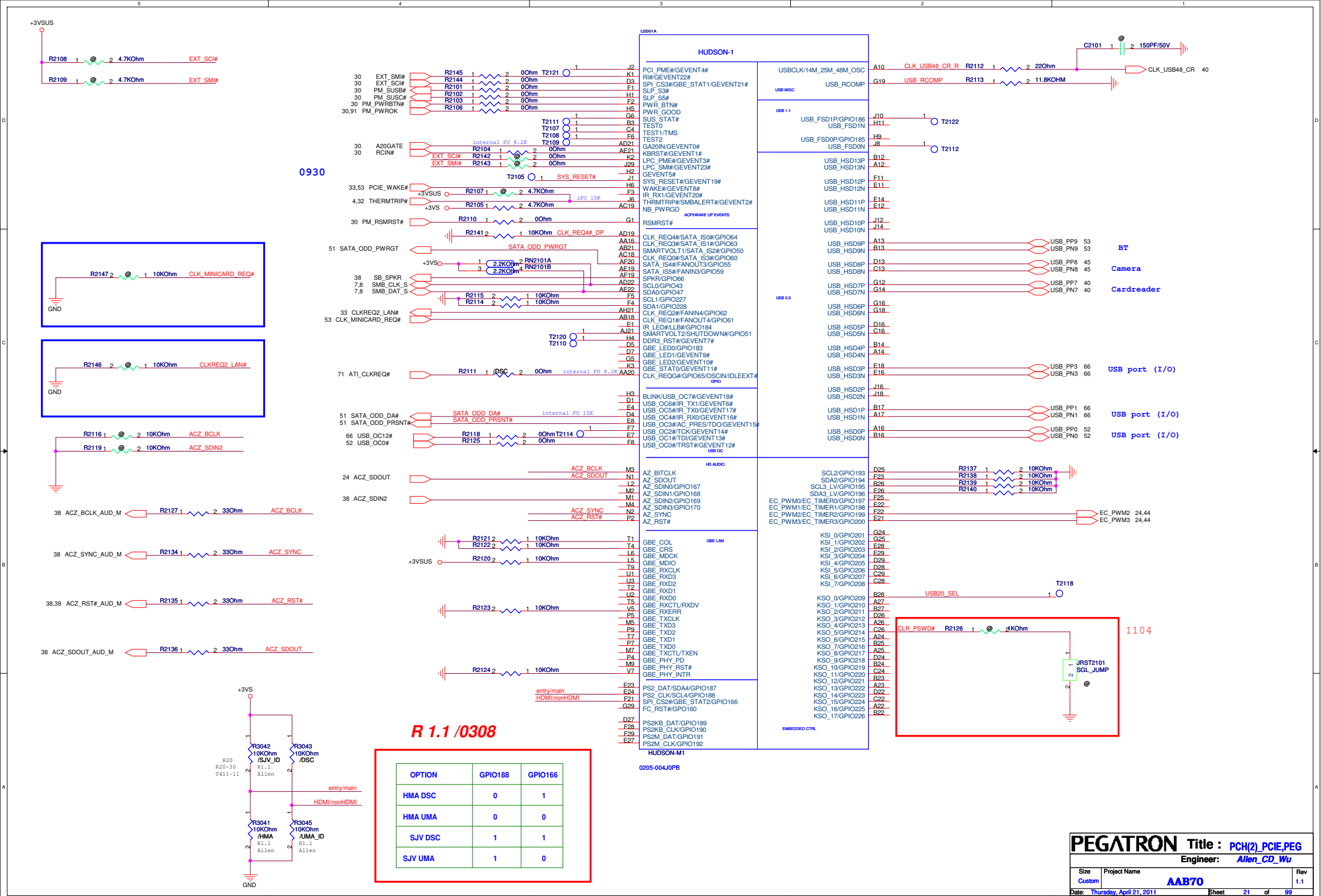
check 0125

BATT_HOLD

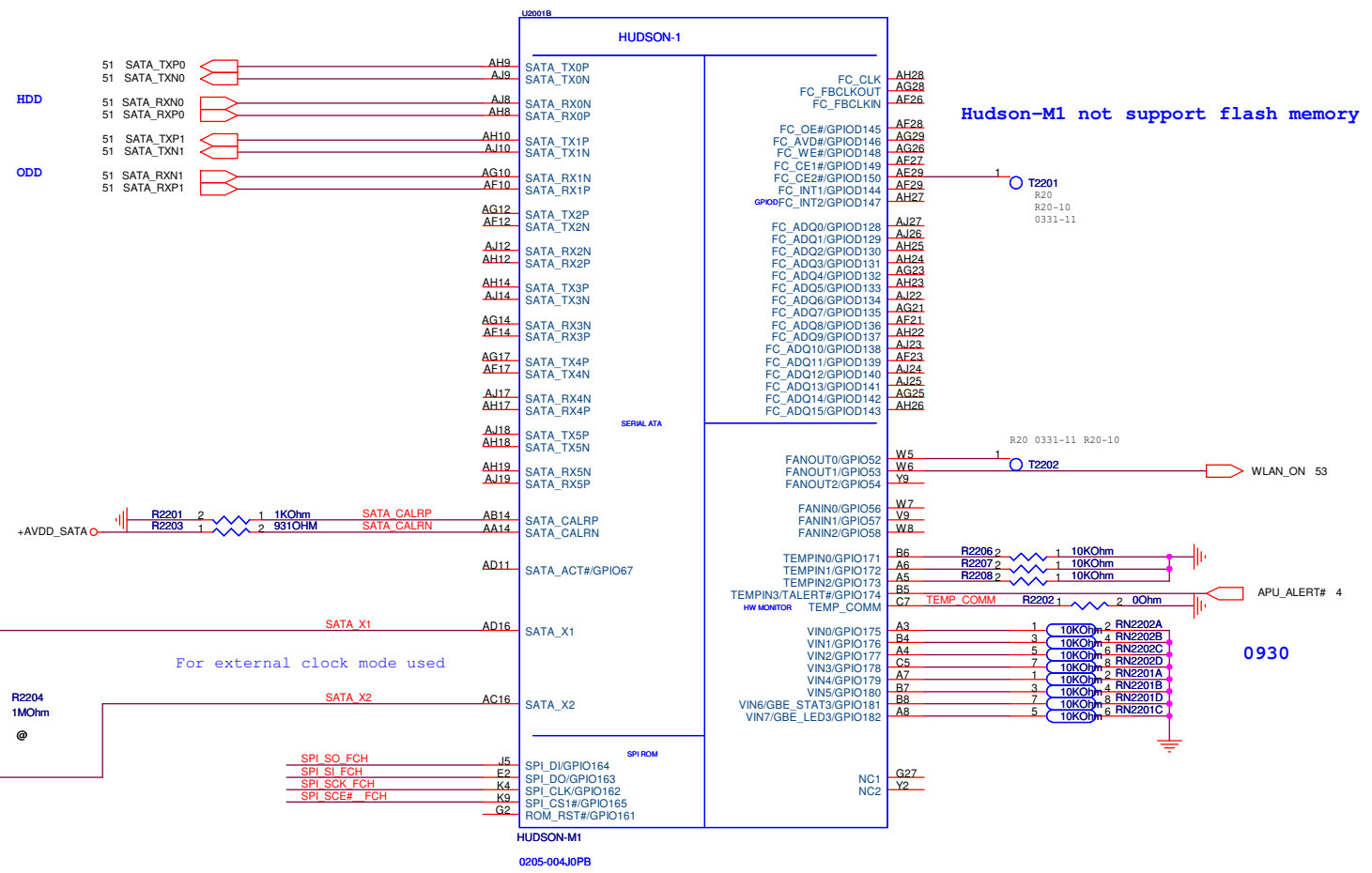
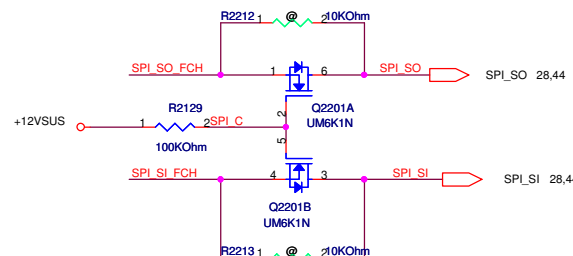
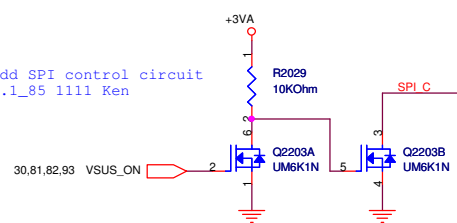
aab70 0120

1221

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

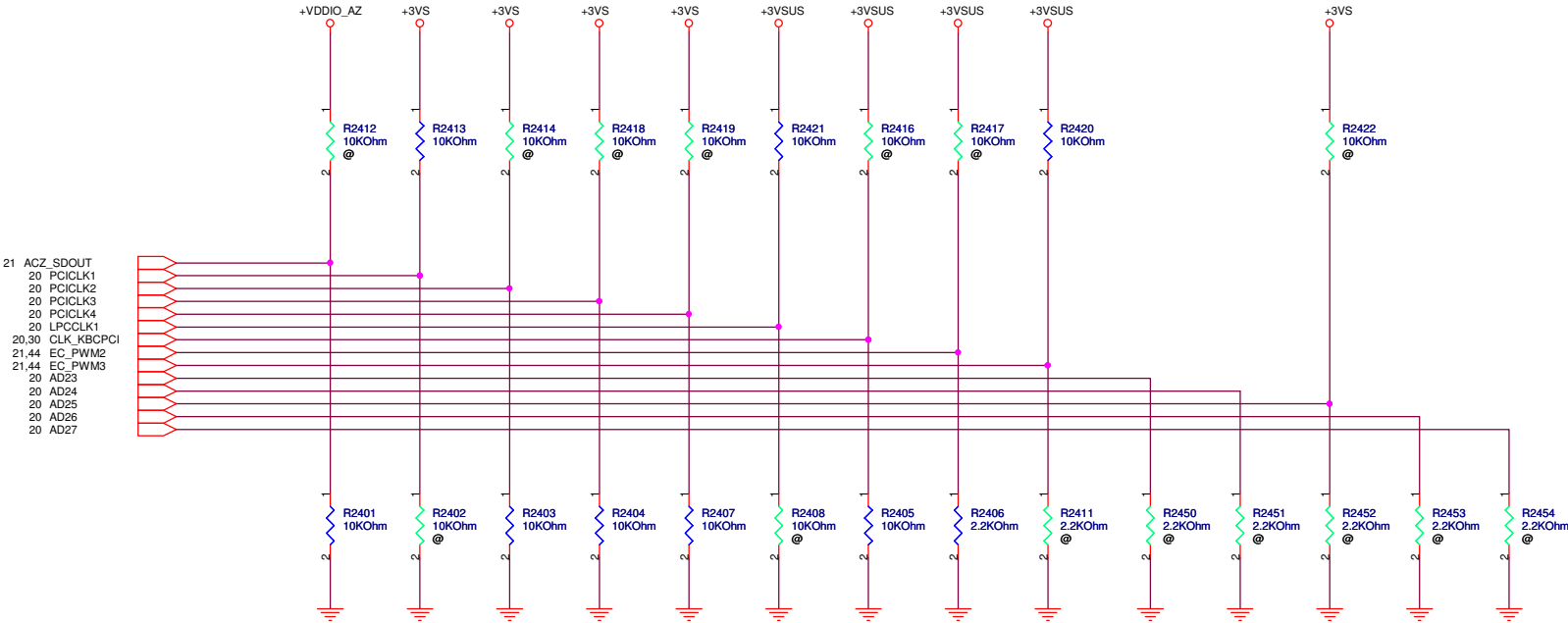


Add SPI control circuit
1.1_85 1111 Ken





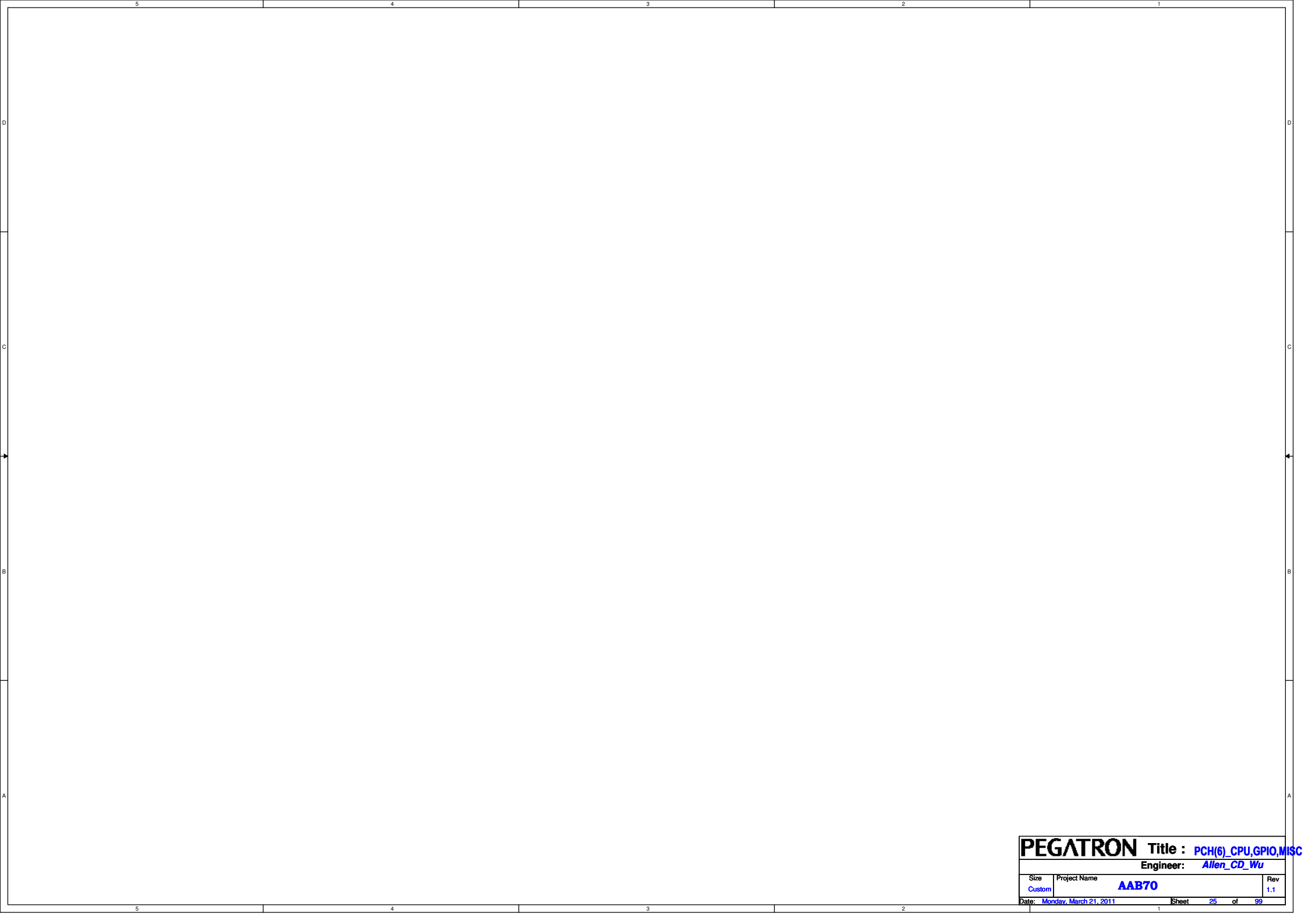
Strap Pins



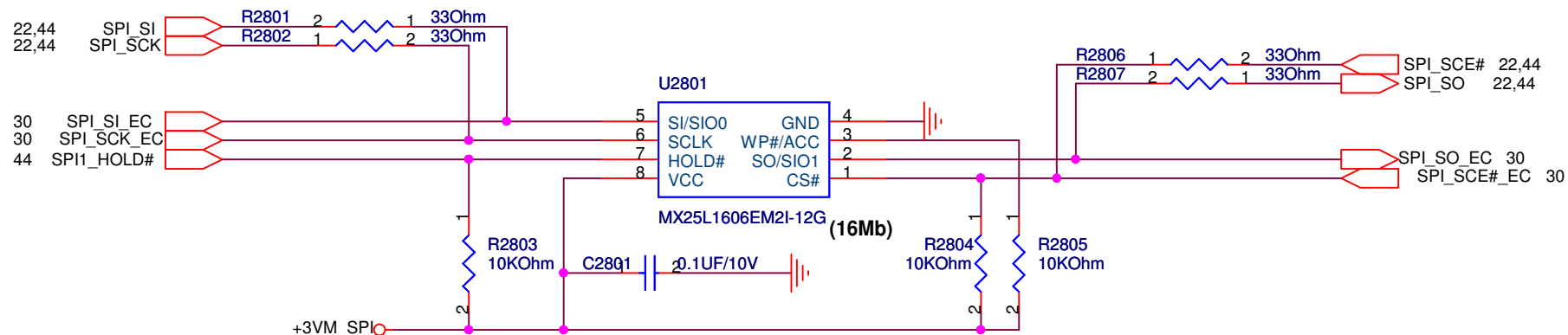
	ACZ_SDOUT_AUD	PCICLK1	PCICLK2	PCICLK3	PCICLK4	LPCCLK0 CLK_KBCPCI	LPCCLK1	EC_PWM2	EC_PWM3	
High	low power mode	PCIE Gen2	watchdog timer enable	debug	no-Fusion clock mode	EC enable	clock gen. enable	H	L	LPC ROM
Low	performance mode	PCIE Gen1	watchdog timer disable	ignore debug	Fusion clock mode	EC disable	clock gen. disable	L	H	SPI ROM

Debug Straps

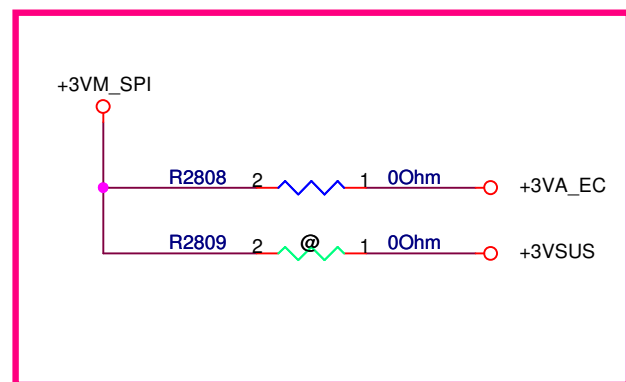
	AD23	AD24	AD25	AD26	AD27
High	disable PCI mem boot	default PCIE straps	use FC PLL	disable ILA autorun	use PCI PLL
Low	enable PCI mem boot	EEPROM PCIE straps	bypass FC PLL	enable ILA autorun	by pass PCI PLL



PEGATRON		Title : PCH(6)_CPU,GPIO,MISC	
		Engineer: Allen_CD_Wu	
Size Custom	Project Name AAB70		Rev 1.1
Date: Monday, March 21, 2011		Sheet 25	of 99



1110

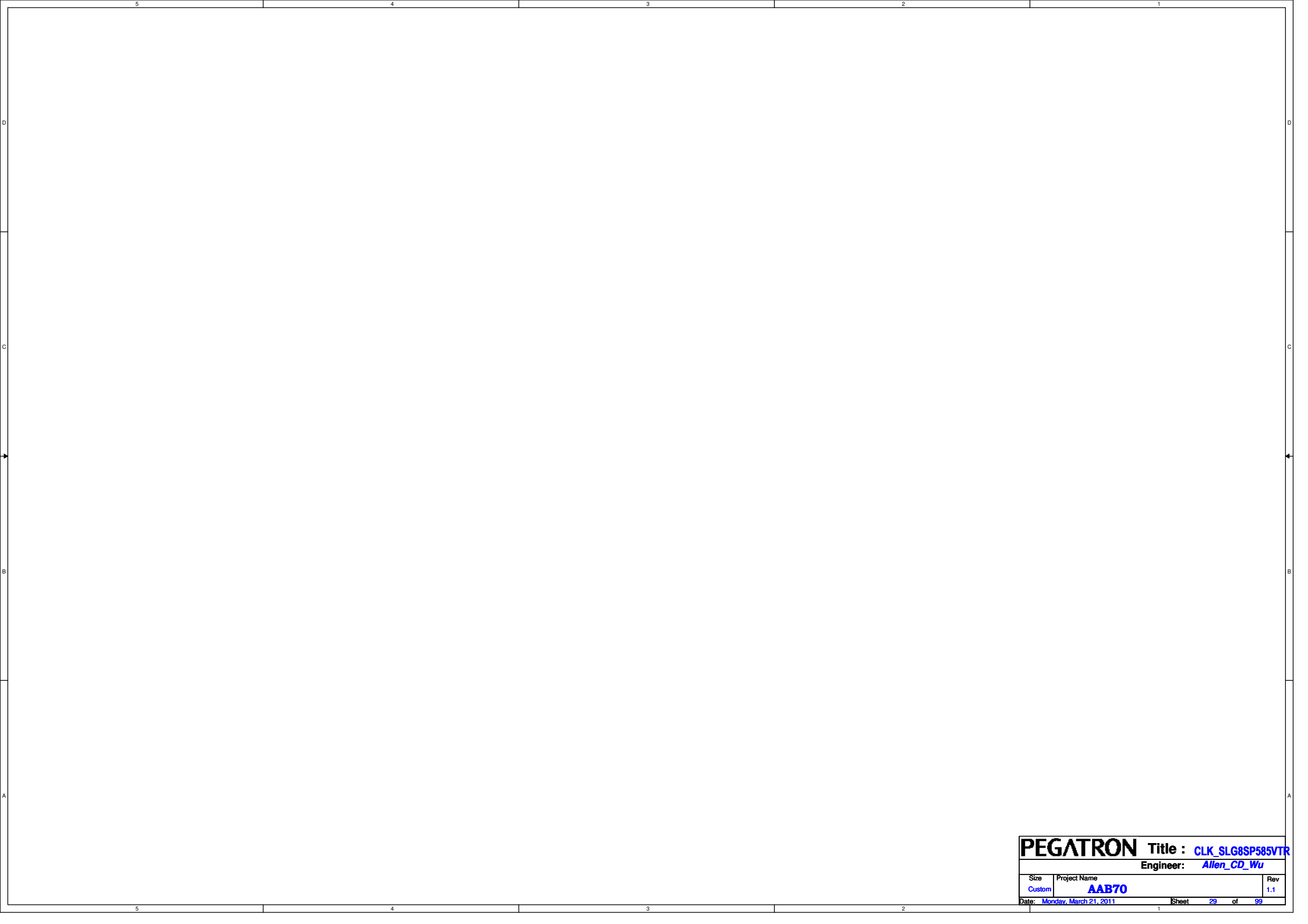


WINBOND: 0500-00P4000

MXIC: 0500-00TY000

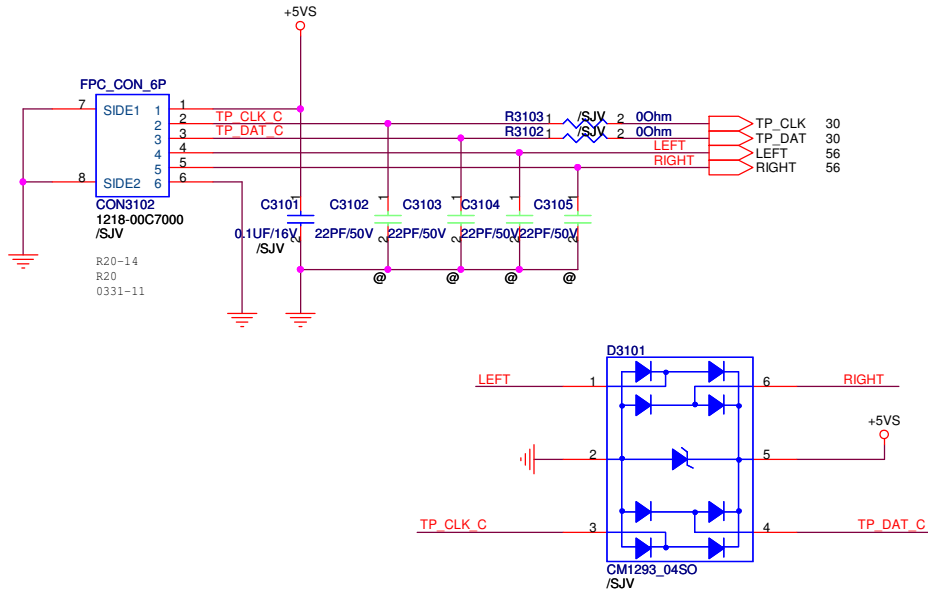
reserved for BIOS testing

PEGATRON		Title : SPI ROM	
		Engineer: Allen_CD_Wu	
Size A	Project Name BS_AB		Rev 1.1
Date: Thursday, April 21, 2011		Sheet 28	of 99

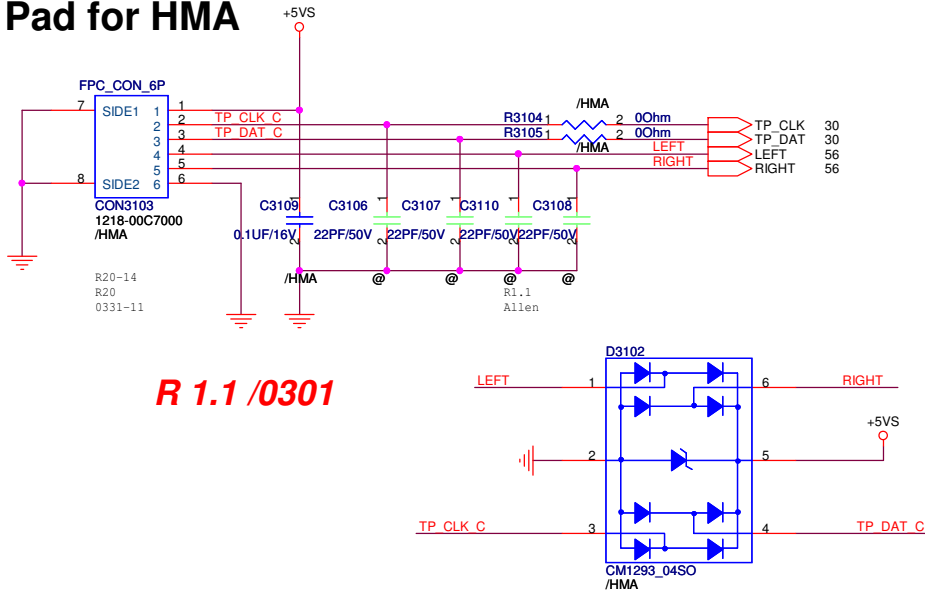


PEGATRON		Title : CLK_SLG8SP585VTR	
		Engineer: Allen_CD_Wu	
Size	Project Name		Rev
Custom	AAB70		1.1
Date: Monday, March 21, 2011		Sheet 29	of 99

Touch Pad for SJV

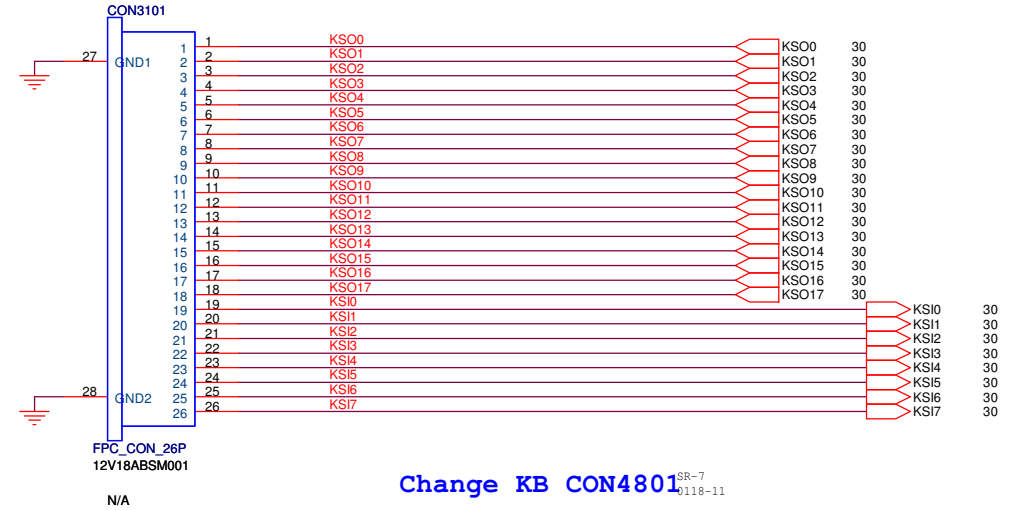


Touch Pad for HMA



Keyboard FOR 17"

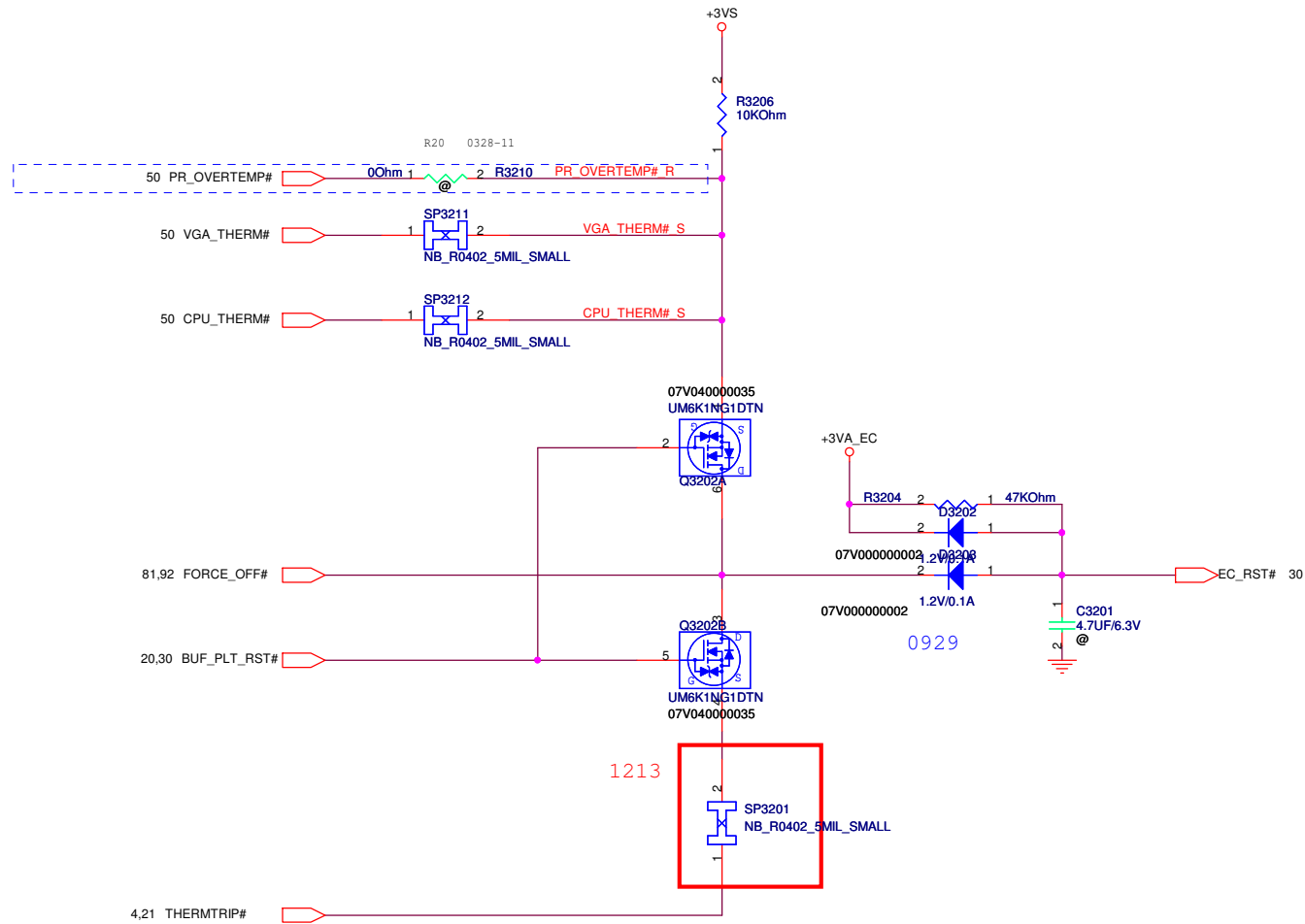
AAB70 0124



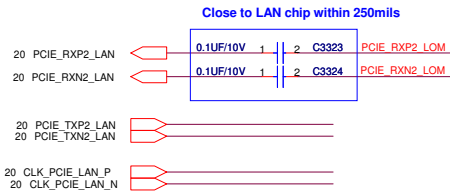
Change KB CON4801^{SR-7}
0118-11

Thermal Policy

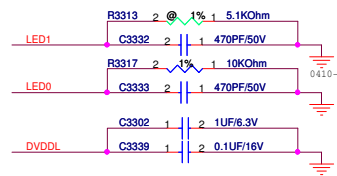
NPCE795 has internal power-on reset circuit
Use 47k ohm to make sure that raising time of POR is less than 10us



PEGATRON			Title : RST_Reset Circuit
			Engineer: Allen_CD_Wu
Size B	Project Name AAB70	Rev 1.1	
Date: Thursday, April 21, 2011		Sheet 32	of 99



Close to LAN chip within 250mils



Modify H/W strap setting

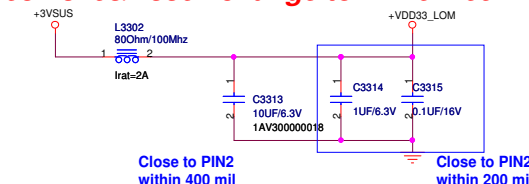
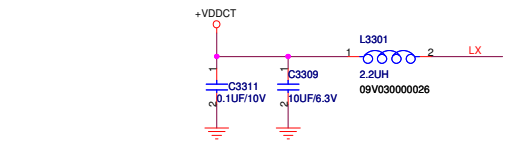
SR-41
0125-11

Powr-on strapping
(1) LED[0]: enable overclocking
pull-high: overclocking (default)
stuff R3326, R3324; Remove R3317, R3325, R3327;
pull-low: un-overclocking
stuff R2, R3325, R3327; Remove R3326, R3324

(2) LED[1]: selection for AR8158's internal VDDCT (SWR/LDO)
pull-high: SWR mode
stuff R3330, R3332; Remove R3313, R3331, R3333;
pull-low: LDO mode
stuff R3313, R3331, R3333; Remove R3330, R3332

R 1.1 /0308 L3403/L3302 change to PB201209T-152-N

AR8158 (SWR mode)
Stuff L3301, C3311, C3309 ; remove C3301, R3311
AR8158 (LDO mode)
Stuff R3311, C3301, C3303 ; Remove L3301, C3311, C3309

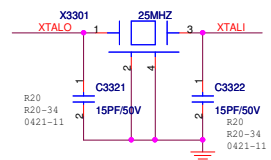


Close to PIN2 within 400 mil

Close to PIN2 within 200 mil

Modify R3311 as VP

SR-31
0125-11



Modify LAN AR8158 circuit

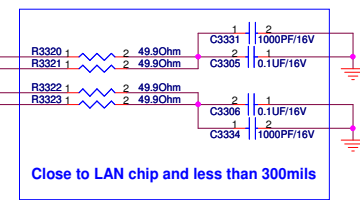
SR-12
0121-11

Change U3301 to AR8158 Part and remover SM BUS

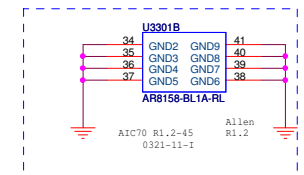
SR-32
0125-11

Remove LAN LED circuit

SR-29
0125-11



Close to LAN chip and less than 300mils

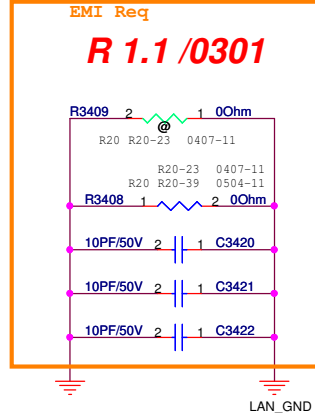
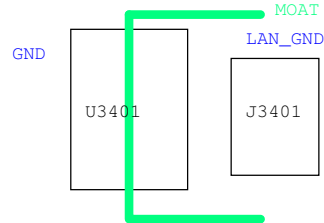


R 1.1 /0308 L3403/L3302 change to PB201209T-152-N

R 1.1 /0308

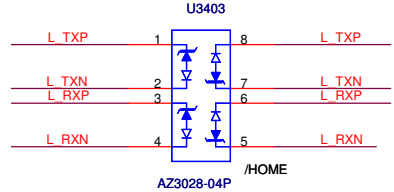
D3401
AZ2025-01H.R7G

LAN layout note:

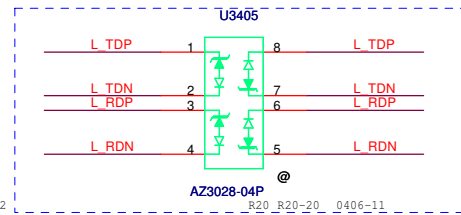


RJ45

Change RJ45 CON3401
0301
1223-0002000
R 1.1 /0301



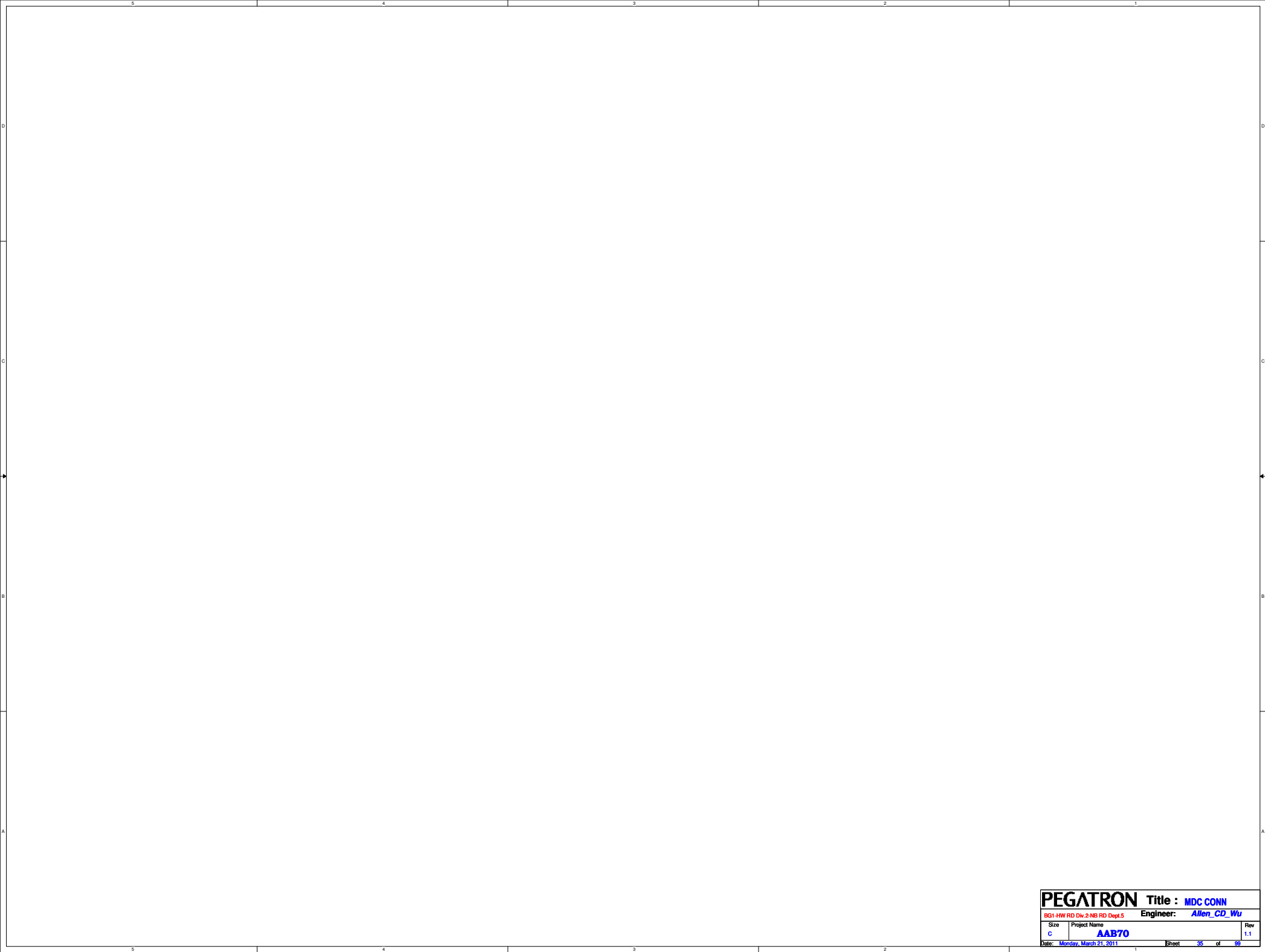
Modify LAN ESD circuit



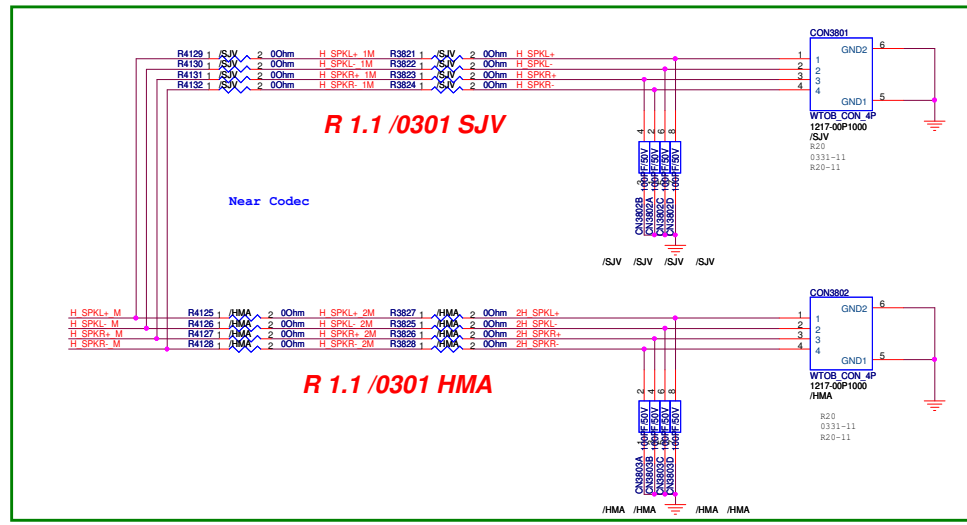
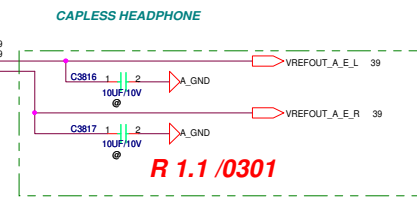
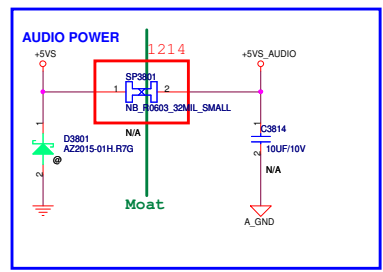
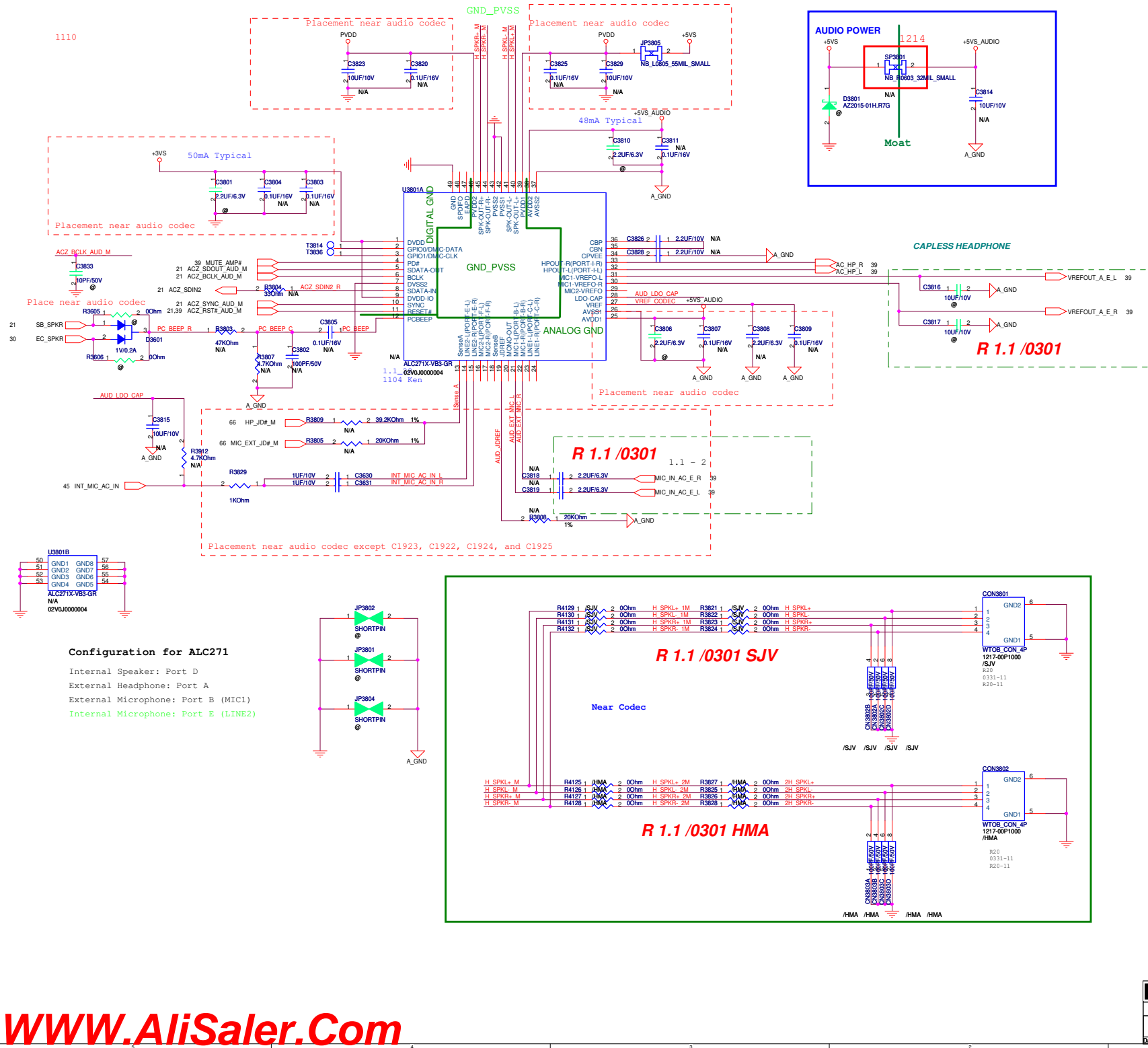
Modify LAN AR8158 circuit

Modify Transformer circuit

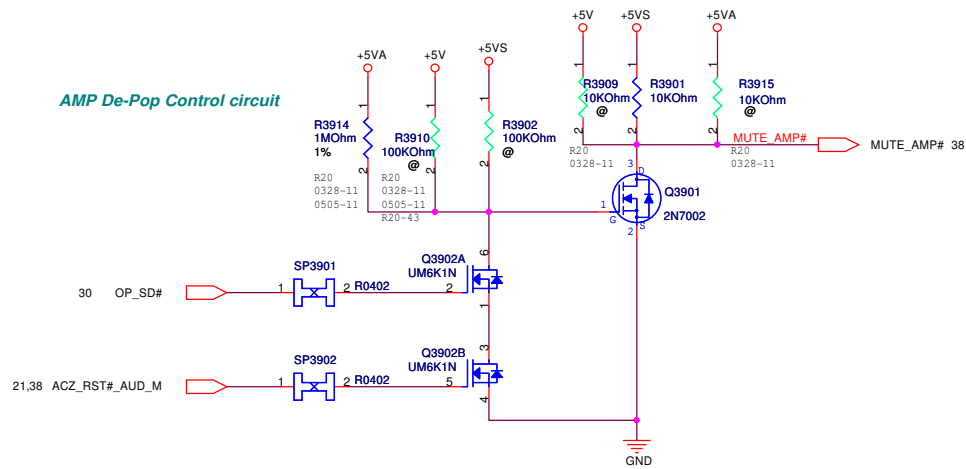
PEGATRON		Title : <u>RJ45</u>	
BG1-HW RD Div.2-NB RD Dept.5		Engineer: <u>Allen_CD_Wu</u>	
Size B	Project Name AAB70	Rev 1.1	
Date: <u>Wednesday, May 04, 2011</u>		Sheet <u>34</u>	of <u>99</u>



PEGATRON		Title : MDC CONN	
BG1-HW RD Dw.2-NB RD Dept.5		Engineer: Allen_CD_Wu	
Size C	Project Name AAB70	Rev 1.1	
Date: Monday, March 21, 2011		Sheet	35 of 99

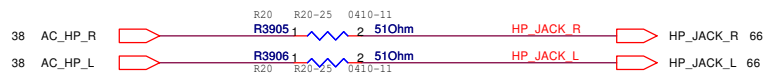
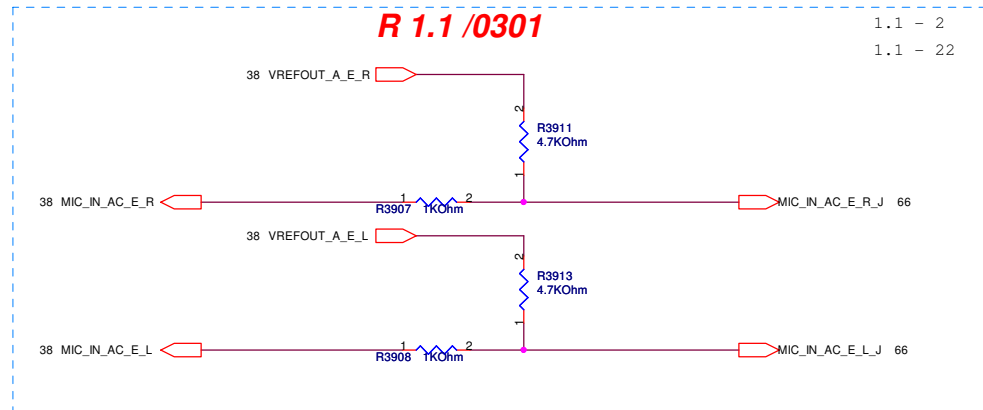


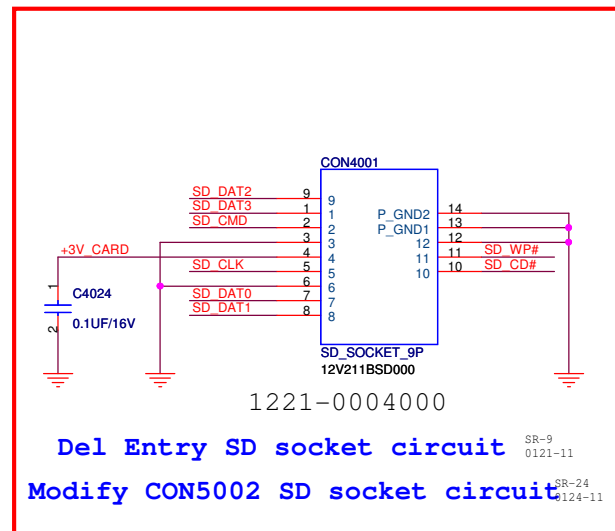
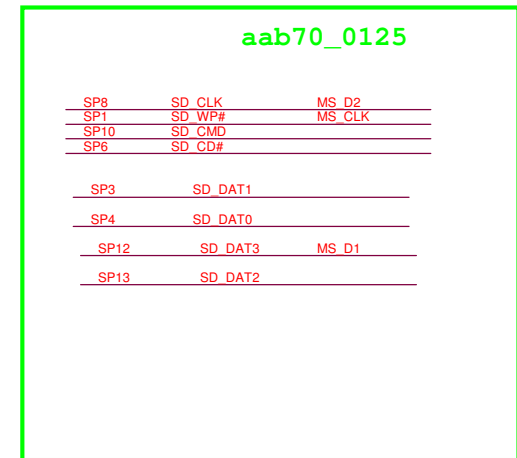
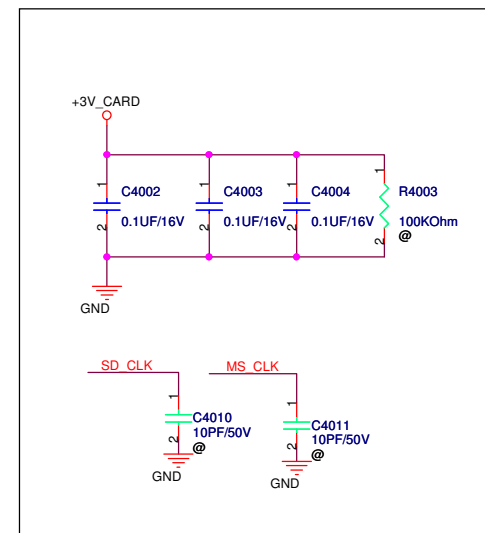
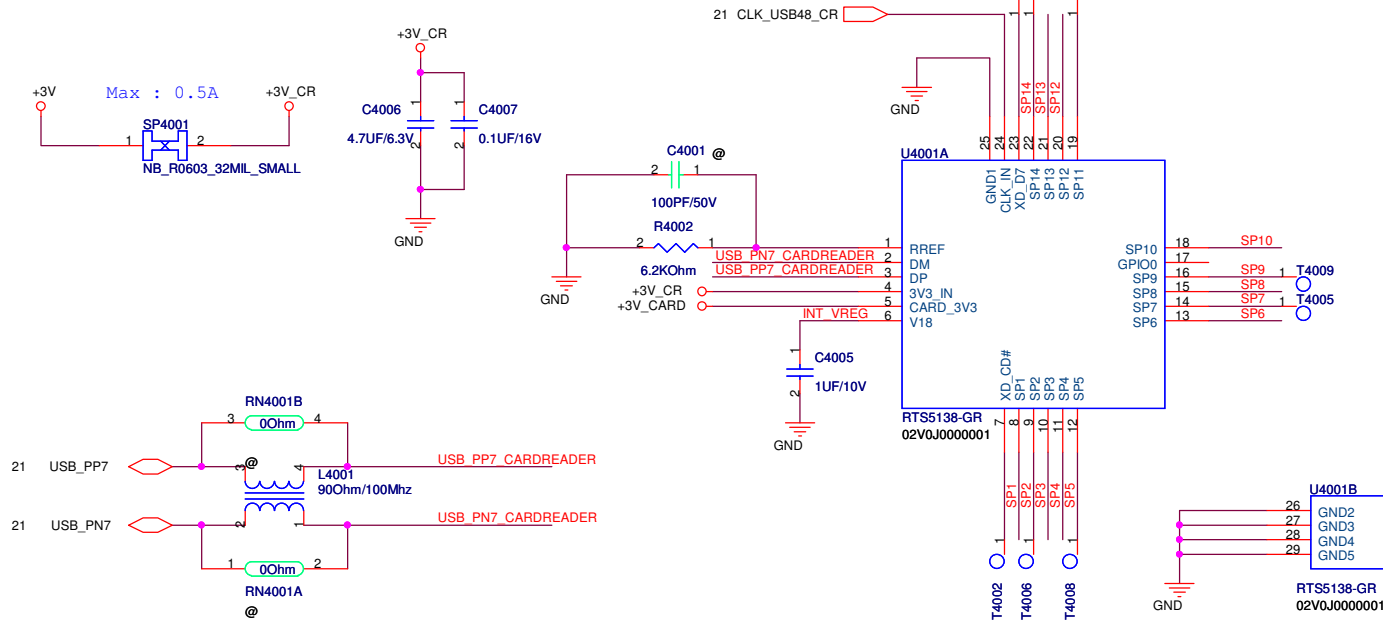
AMP De-Pop Control circuit



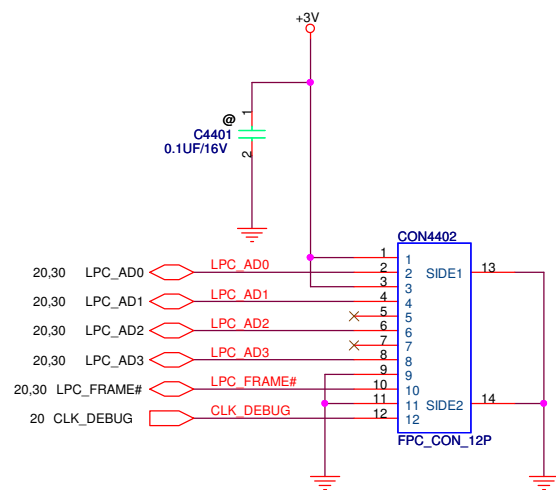
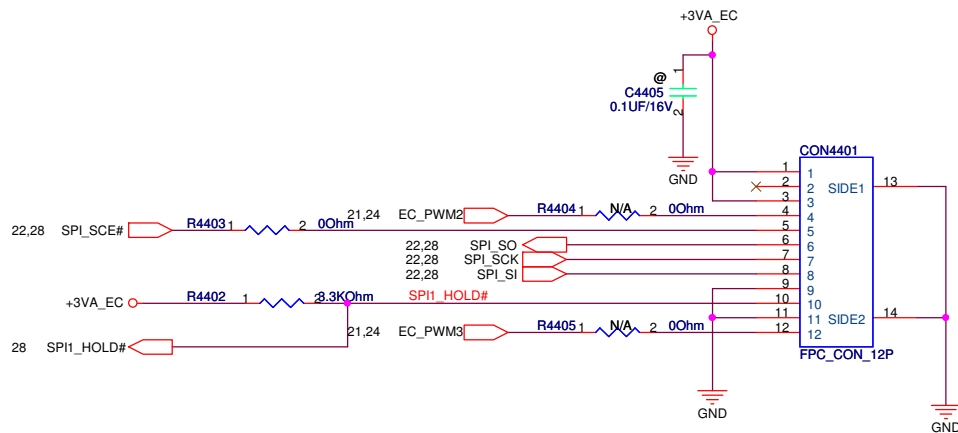
R 1.1 /0301

1.1 - 2
1.1 - 22

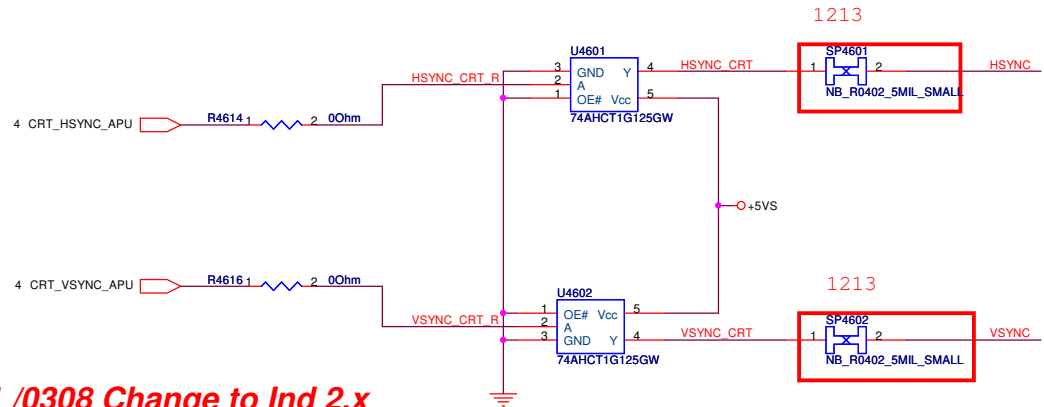
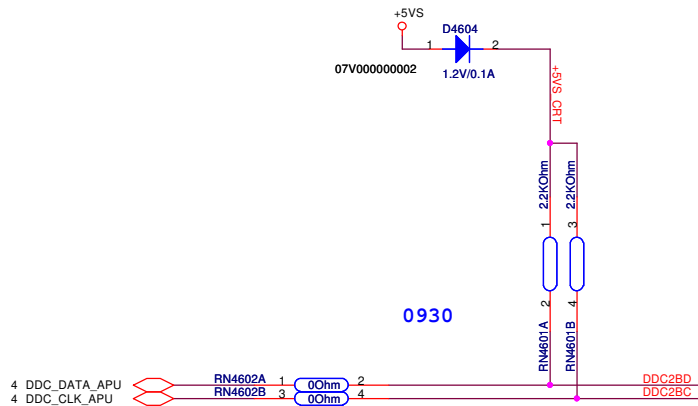




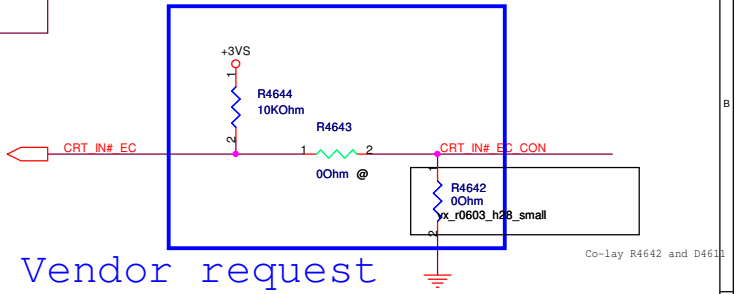
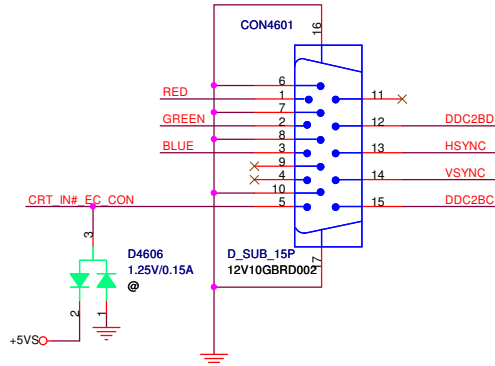
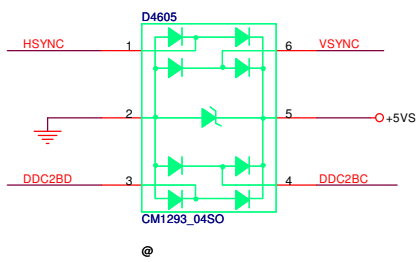
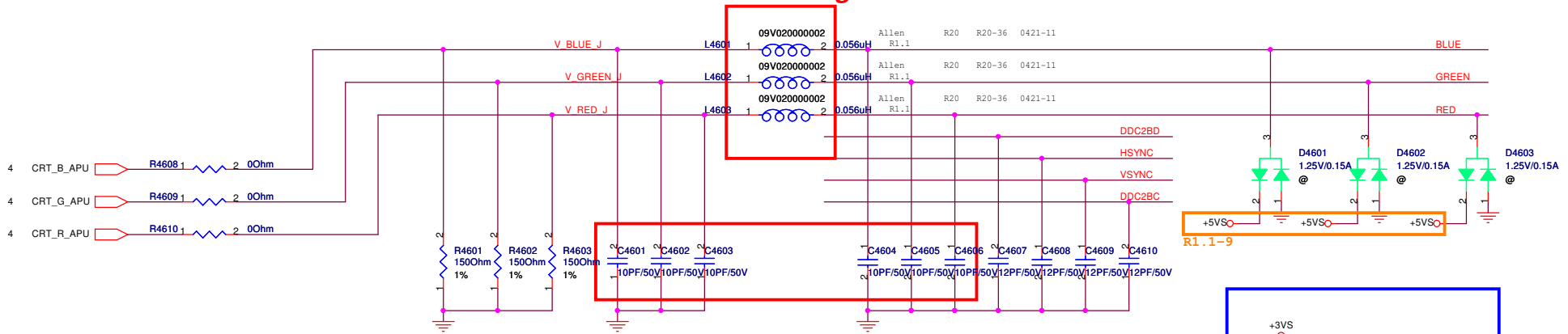
PEGATRON		Title : RTS 5138	
PEGATRON CORPORATION		Engineer:	
Size B	Project Name AAB70	Rev 1.1	
Date: Thursday, April 21, 2011		Sheet 40 of 99	



PEGATRON		Title : DEBUG	
BG1/HW2		Engineer: Allen CD Wu	
Size B	Project Name AAB70	Rev 1.1	
Date: Thursday, April 21, 2011		Sheet 44 of 99	

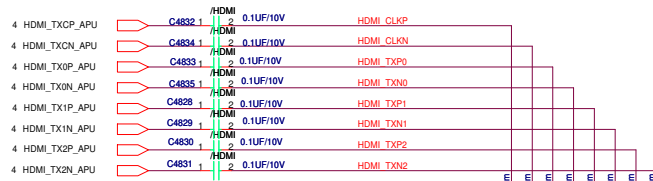


R 1.1 /0308 Change to Ind 2.x

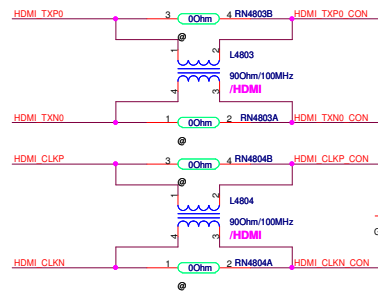
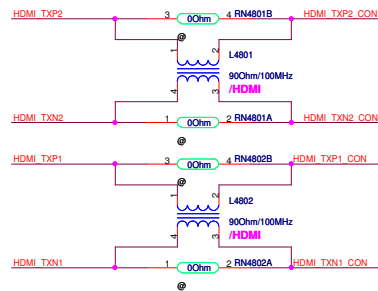
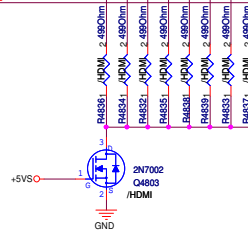
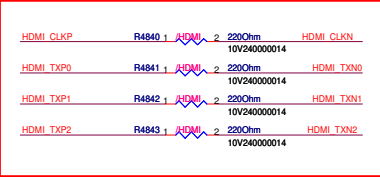


1210-00DY000

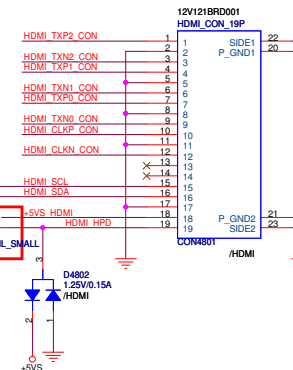
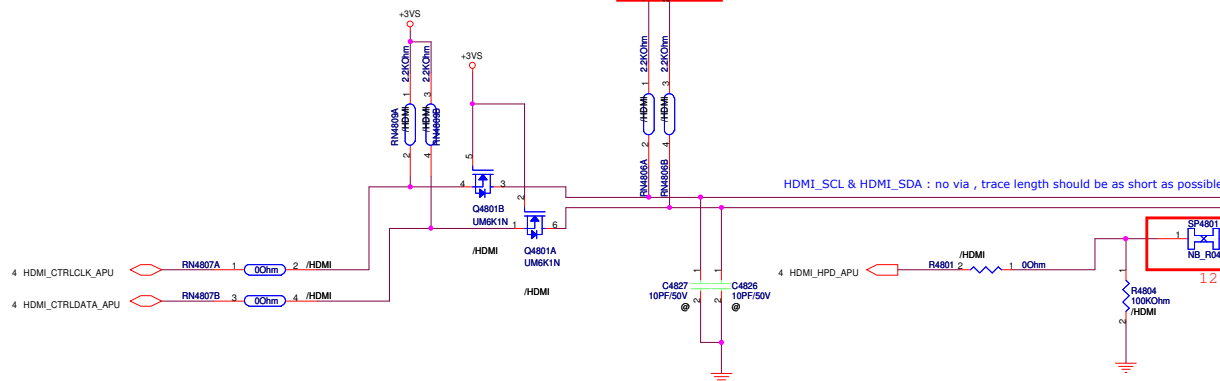
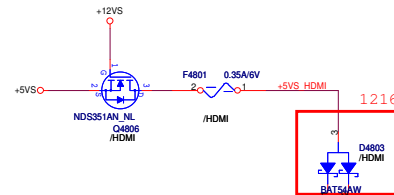
PEGATRON		Title : CRT	
BG1/HW2		Engineer: Allen CD Wu	
Size Custom	Project Name AAB70		Rev 1.1
Date: Thursday, April 21, 2011		Sheet 46 of 99	



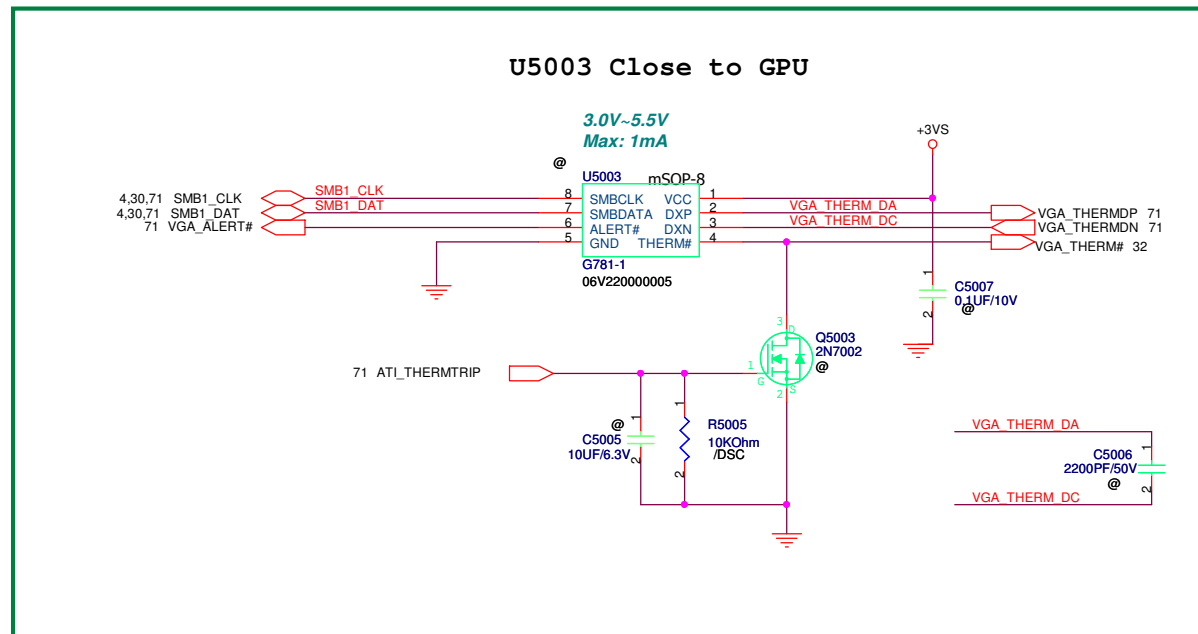
1223



R 1.1 /0301



The diagram shows the U5001 temperature sensor (G709T1U1F, 06V220000007) connected to the CPU_THERM# 32 pin. The sensor's VCC (pin 5) is connected to +3VS, and its GND (pin 4) is connected to ground. A 0.1uF/10V capacitor (C5004) is connected between VCC and GND. The sensor's SET (pin 1) and HYST (pin 2) pins are connected to the THERM SET pin (pin 1) of the R5001 resistor network. The CPU_THERM# (pin 3) is connected to the CPU_THERM# 32 pin. The R5001 network consists of a 39KOhm resistor (R20) and a 10V220000066 resistor (R20-32, 0421-11) connected in series between the THERM SET pin and ground.



FAN

1213

SP5001
NB_R0402 5MIL SMALL

C5008
22PF/25V
@

C5003
100PF/50V
@

SS0520

FANQ_TACH 30

WTOB_CON_3P
SIDE2 3
SIDE1 1
CON5001

+5VS

C5011
22PF/25V
@

C5010
2.2UF/10V

C5009
2.2UF/10V

FAN_PWR

CTL_FAN

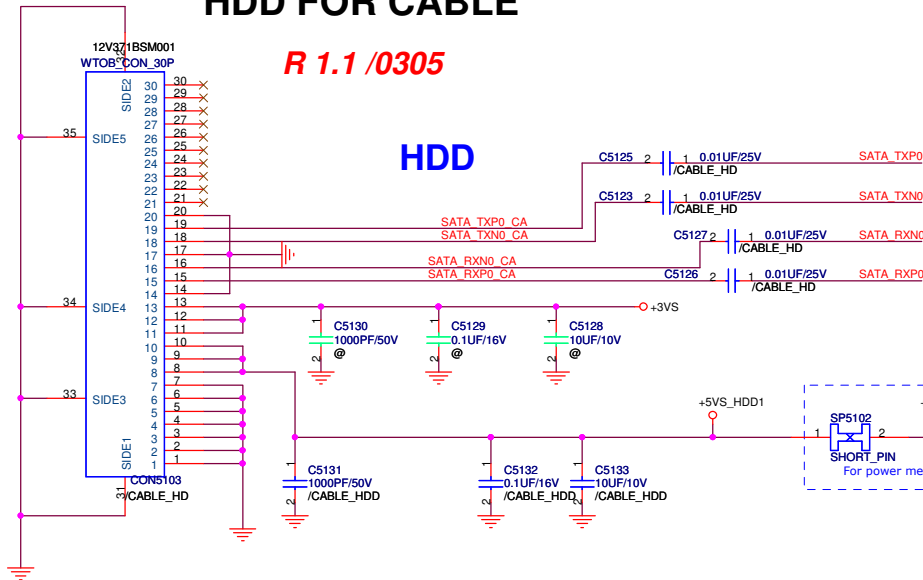
U5002
G991P11U
1 FON# GND4
2 VIN GND3
3 VO GND2
4 VSET GND1
8
7
6
5

[illegible]

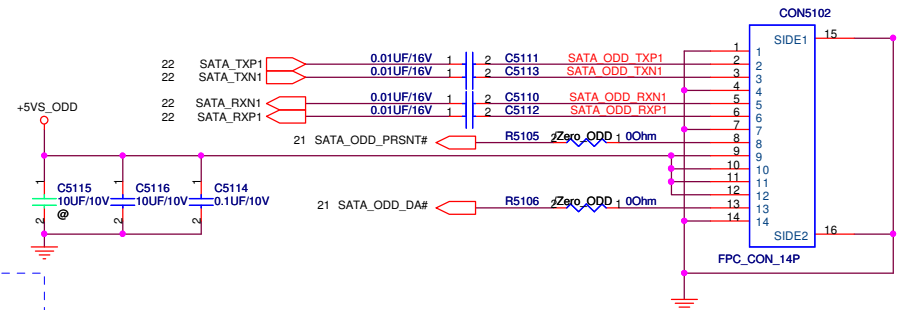
HDD FOR CABLE

R 1.1 /0305

HDD

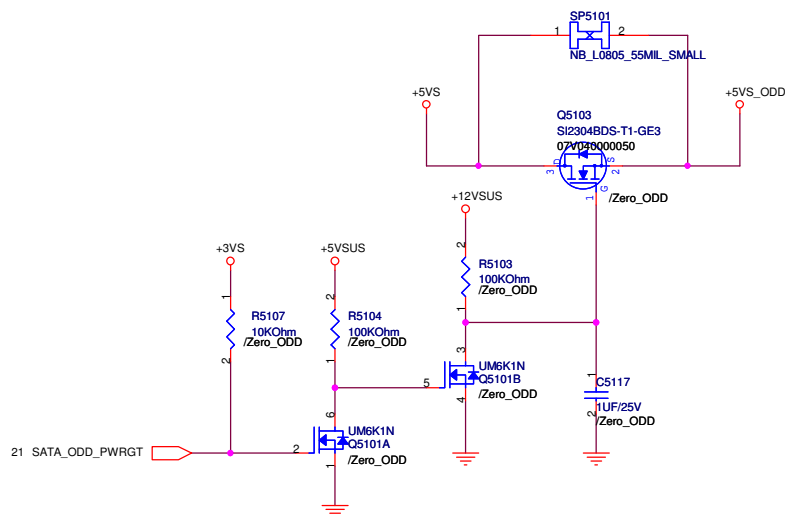


ODD FOR 17"

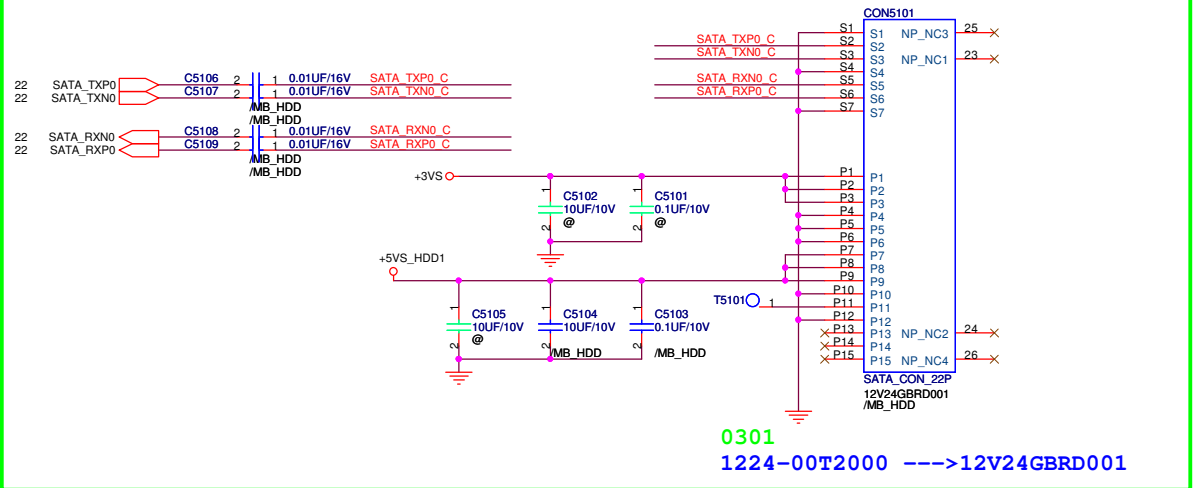


ZERO POWER ODD SUPPORT

support Hokey turn off ODD power



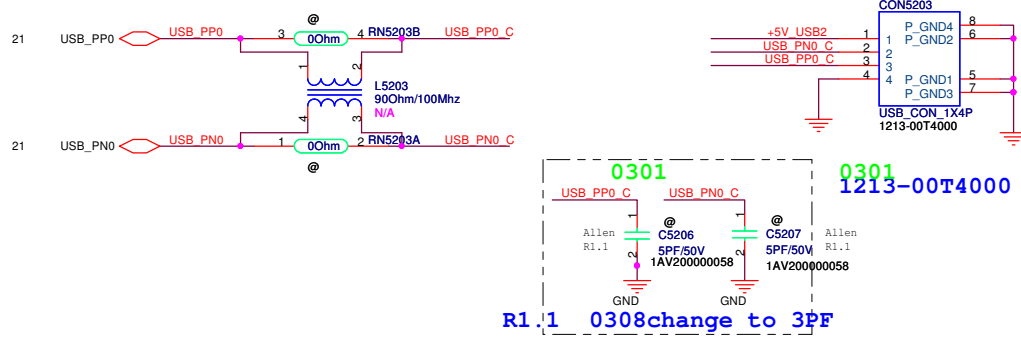
HDD 0129



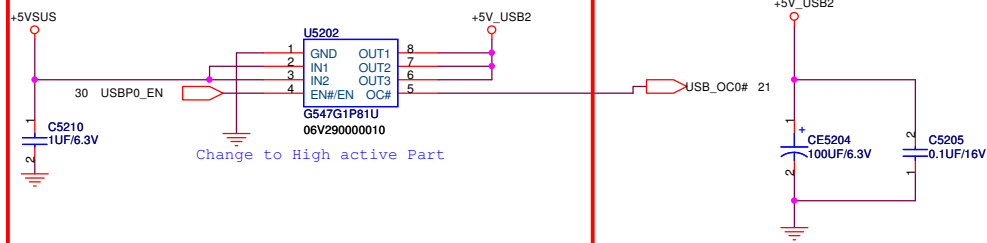
0301
1224-00T2000 --->12V24GBRD001

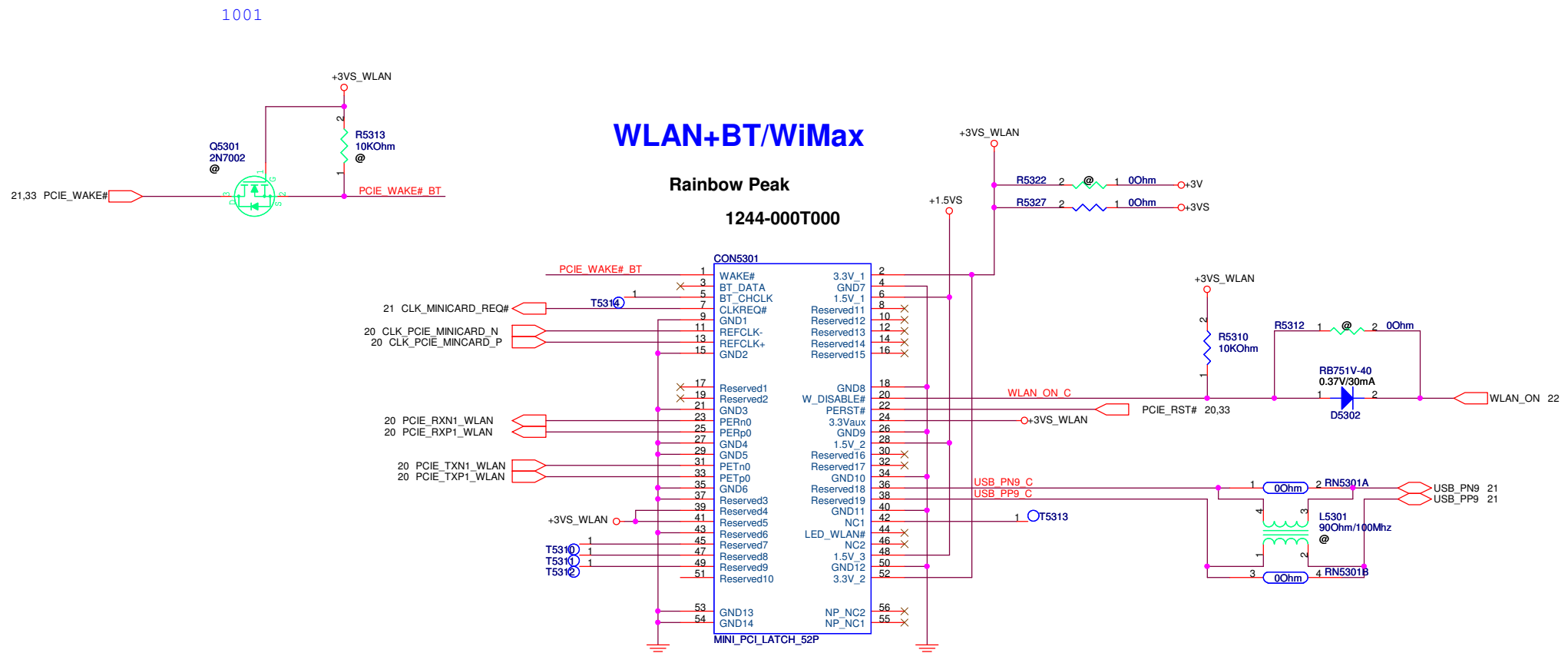
PEGATRON		Title : HDD & CD-ROM	
BG1/HW2		Engineer: <i>Allen CD Wu</i>	
Size	Project Name		Rev
Custom	AAB70		1.1
Date: Thursday, April 21, 2011		Sheet	51 of 99

USB 2.0



AAB70

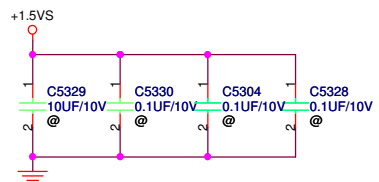




H = 6.5 mm

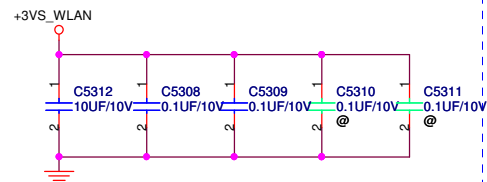
WLAN +1.5VS bypass capacitor:

Place 0.1uF near pin 6,28,48.
Place 10uF near +1.5VS source side.

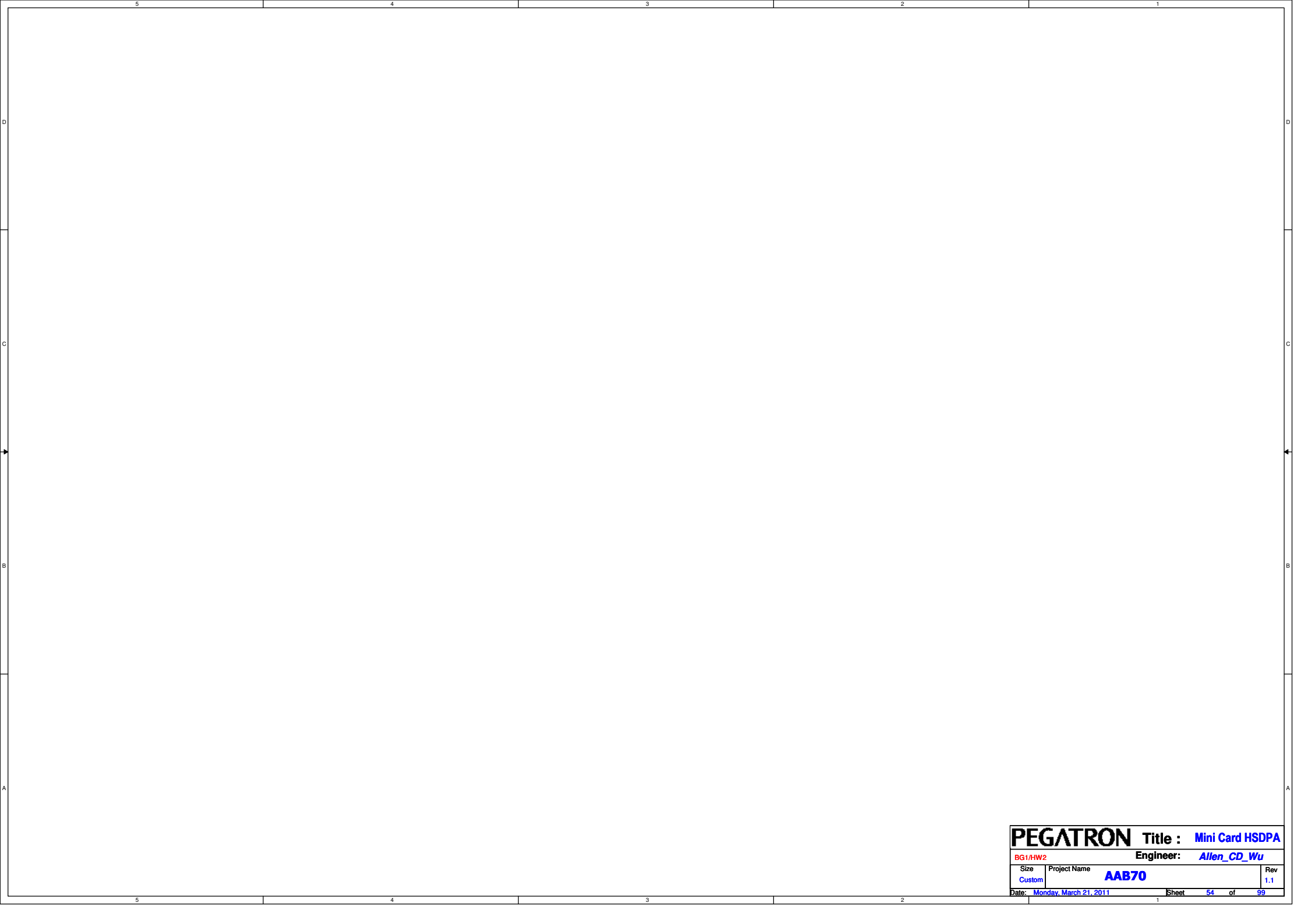


WLAN +3VS bypass capacitor:

Place 0.1uF near pin 2,24,52,39 41.
Place 10uF near +3VS_WLAN source side.

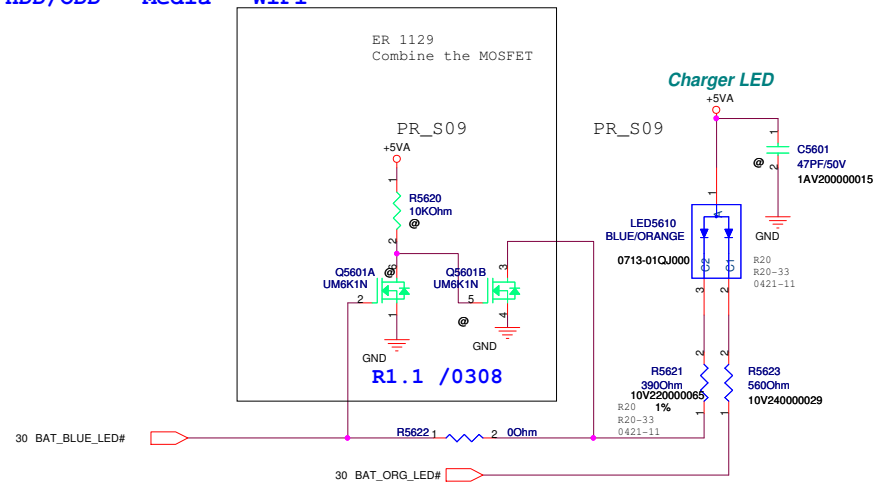


PEGATRON		Title : MINICARD Wireless	
BG1/HW2		Engineer: Allen CD Wu	
Size B	Project Name AAB70		Rev 1.1
Date: Thursday, April 21, 2011		Sheet 53 of 99	

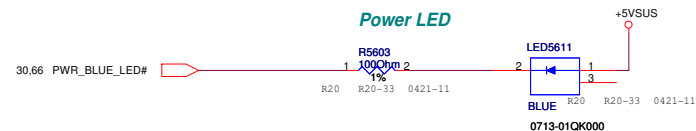


PEGATRON		Title : Mini Card HSDPA	
BG1/HW2		Engineer: Allen_CD_Wu	
Size Custom	Project Name AAB70		Rev 1.1
Date: Monday, March 21, 2011		Sheet 54 of 99	

Order of Indicator LEDs
DC-IN Power Battery HDD/ODD Media WiFi



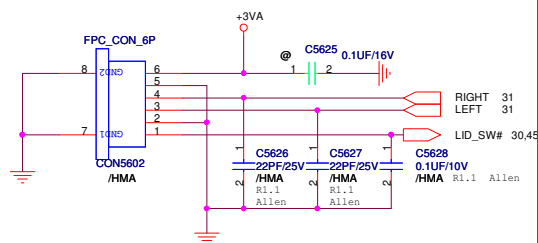
Dual Color



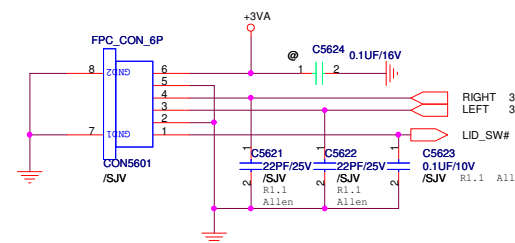
1.1

R 1.1 /0301

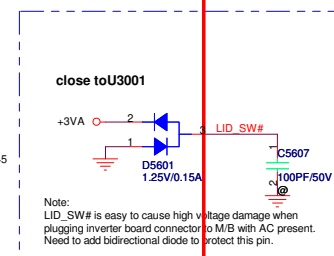
For HMA



For SJV

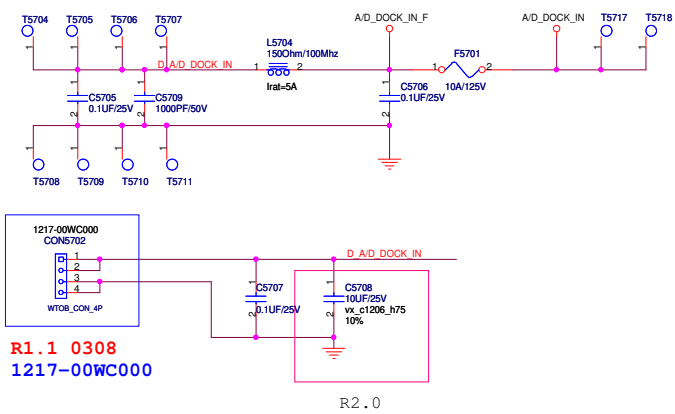


1028

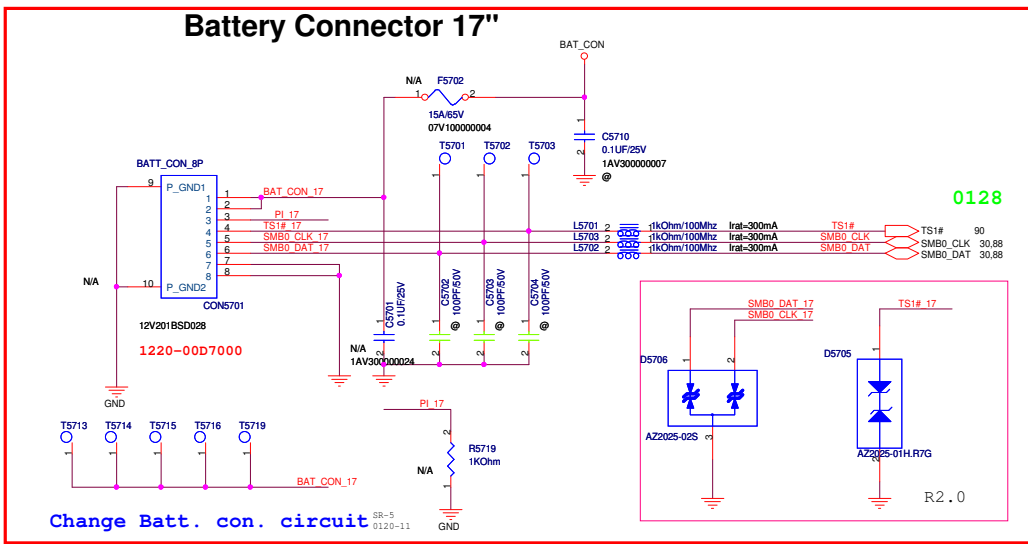


PEGATRON		Title : LED CIR/ FW SCREW	
BG1-HW RD Div.2-NB RD Dept.5		Engineer: Allen_CD_Wu	
Size	Project Name		Rev
Custom	AAB70		1.1
Date: Thursday, April 21, 2011	Sheet	56	of 99

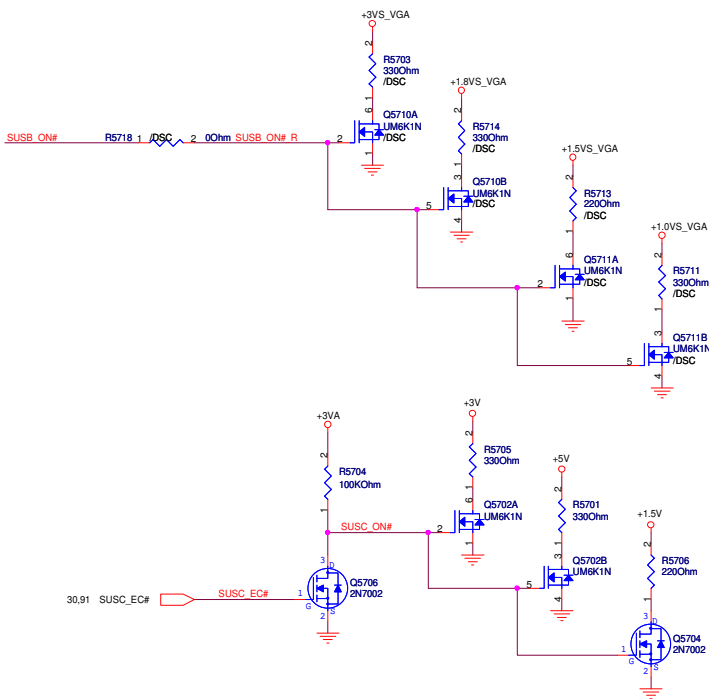
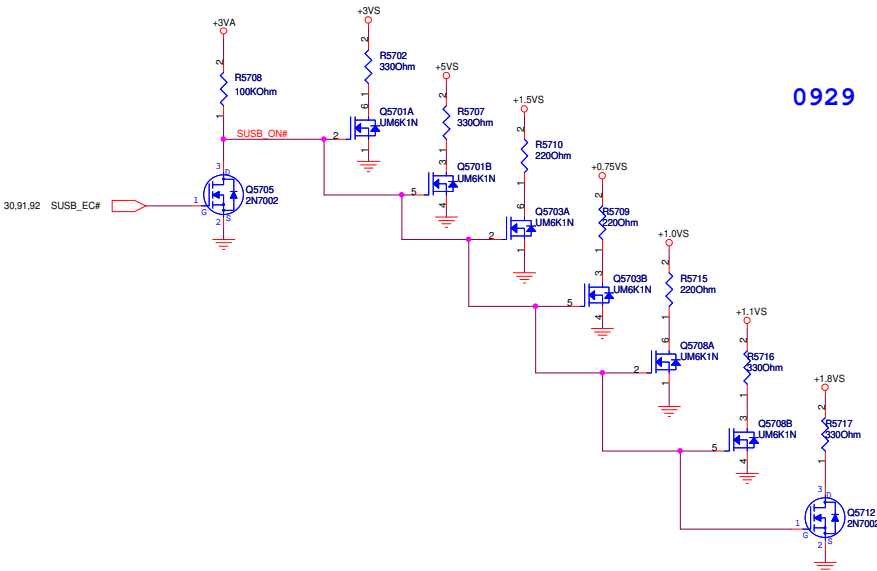
DC IN

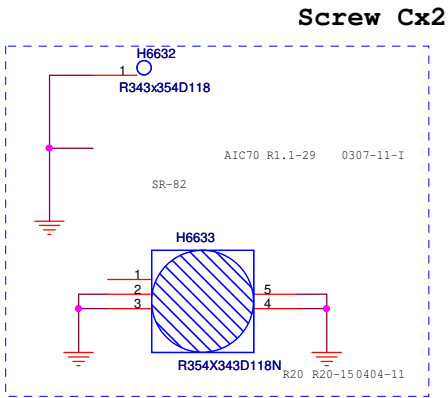
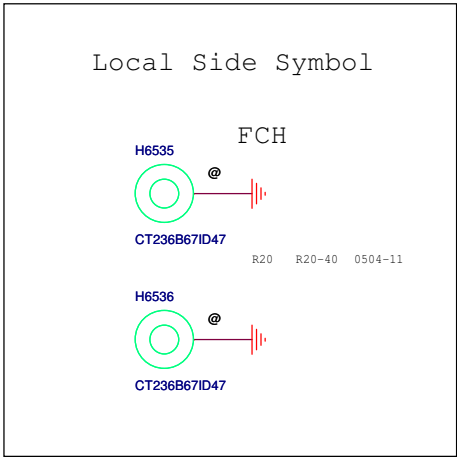
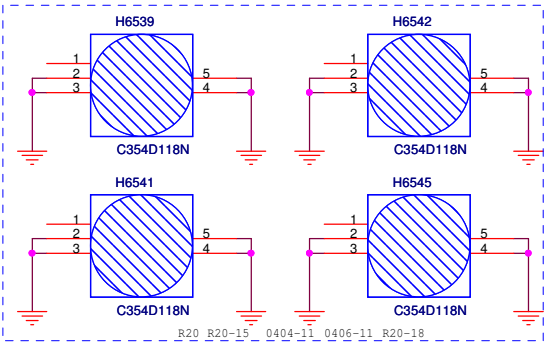
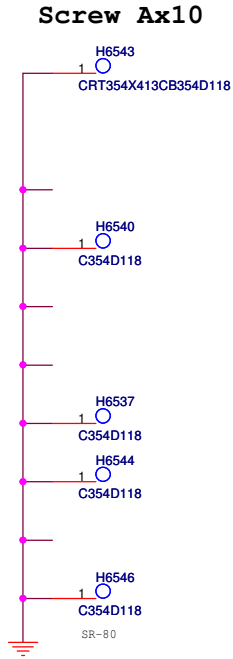
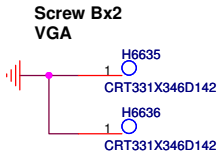
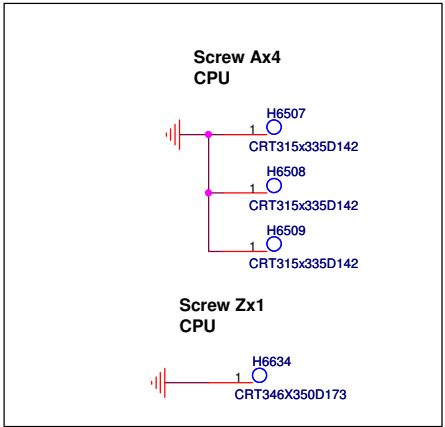
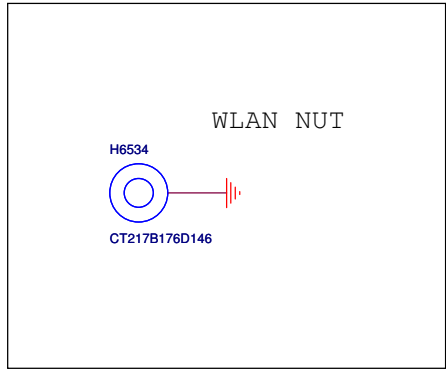


Battery Connector 17"



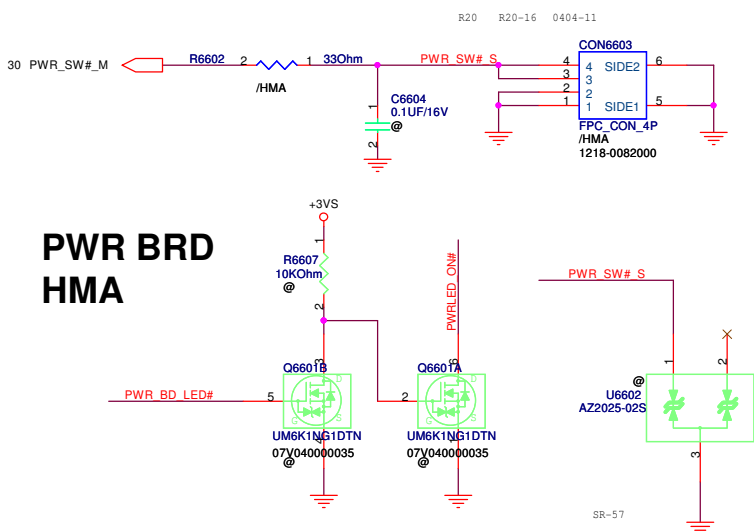
Discharge Circuit





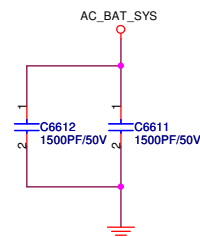
PEGATRON			Title : ME_CONN,Skew Hole	
			Engineer: Allen_CD_Wu	
Size B	Project Name AAB70			Rev 1.1
Date: Wednesday, May 04, 2011		Sheet 65 of 99		

**PWR BRD
HMA**



change PWR LED CON6603 circuit 0129

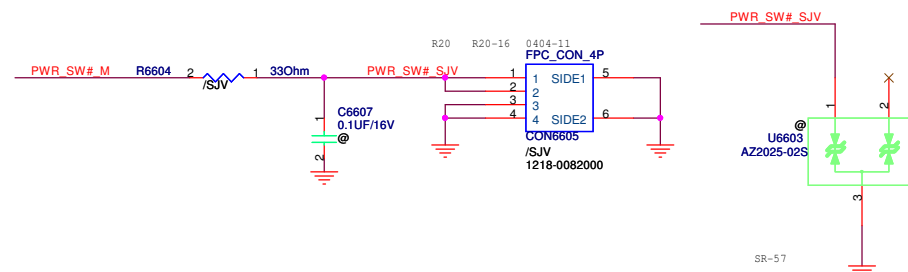
EMI



ADAPTOR VOLTAGE DETECTOR.

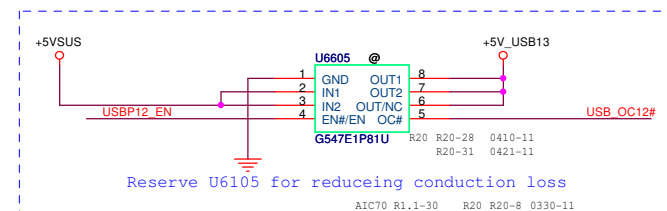
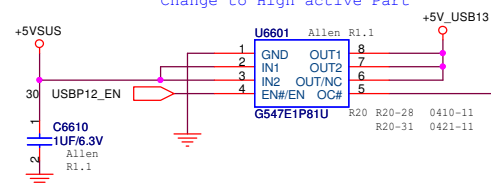
PWR SJV

R 1.1 /0301

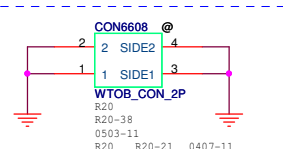
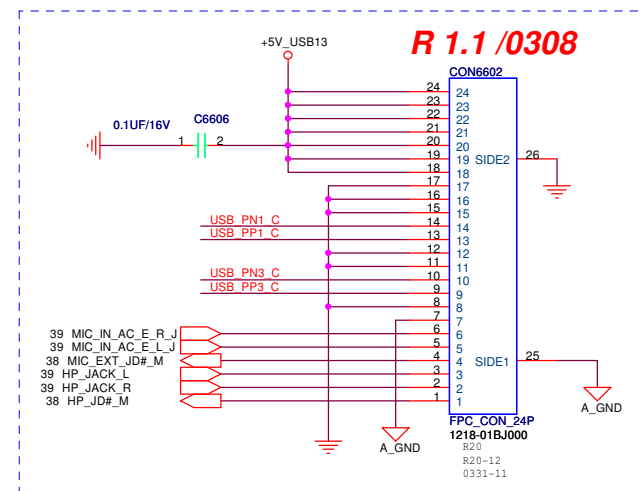
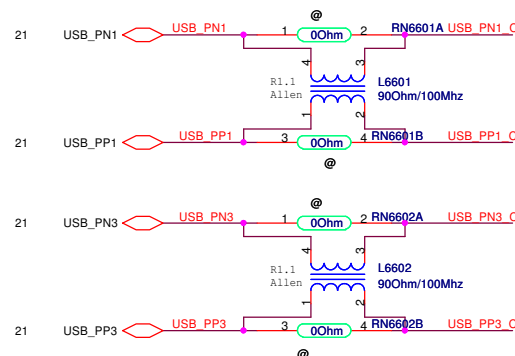


AAB70

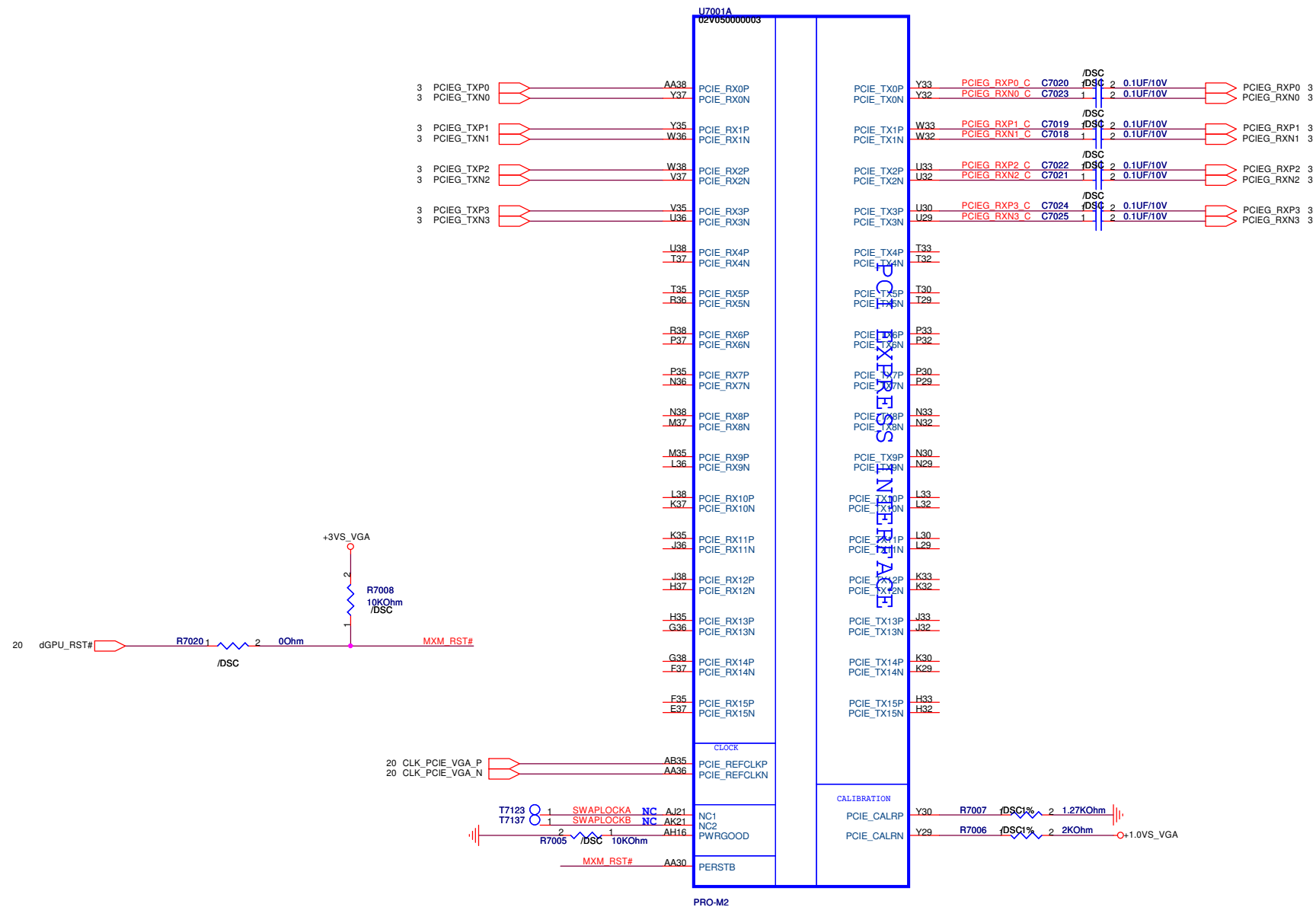
Change to High active Part

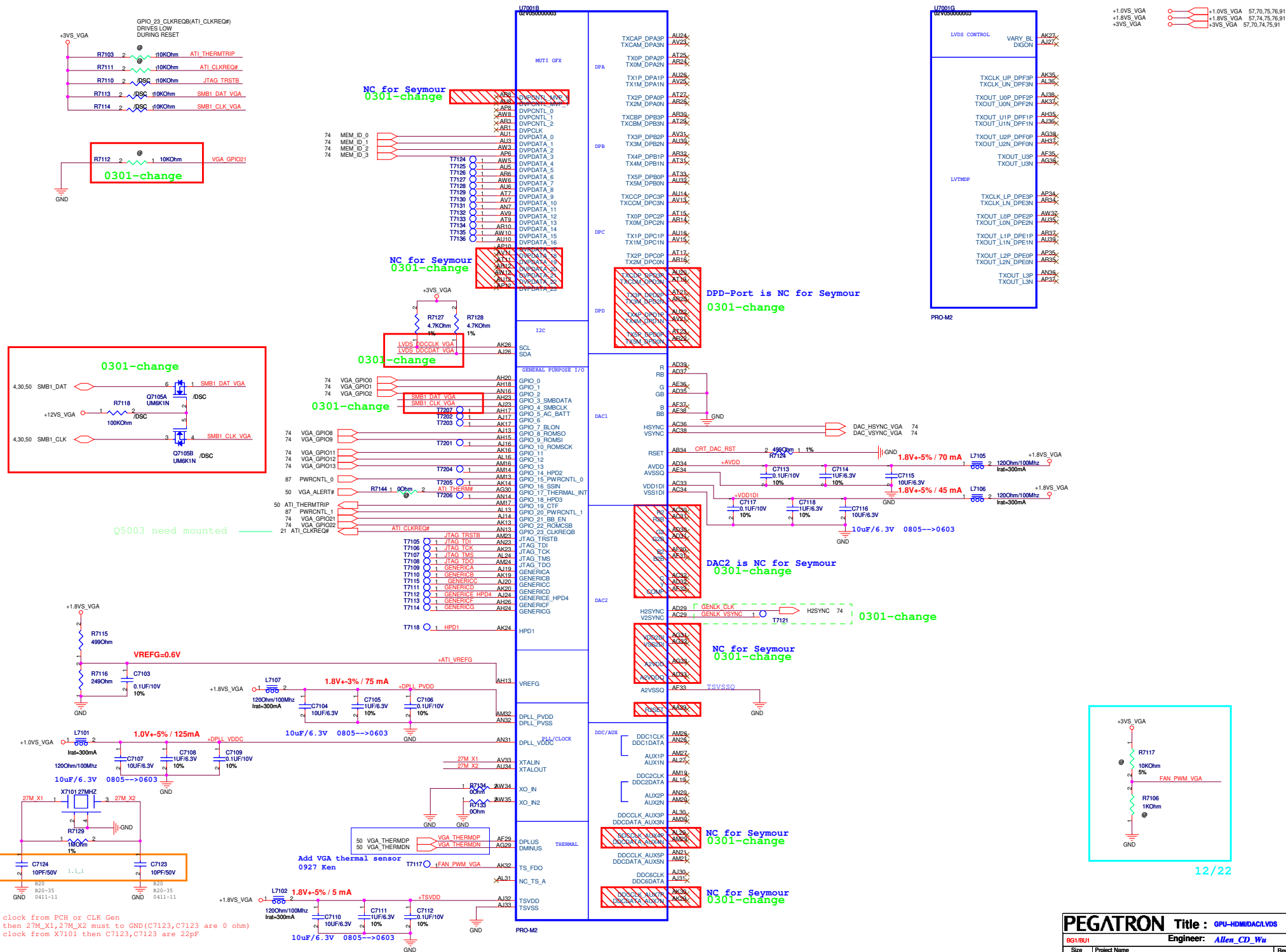


R 1.1 /0308



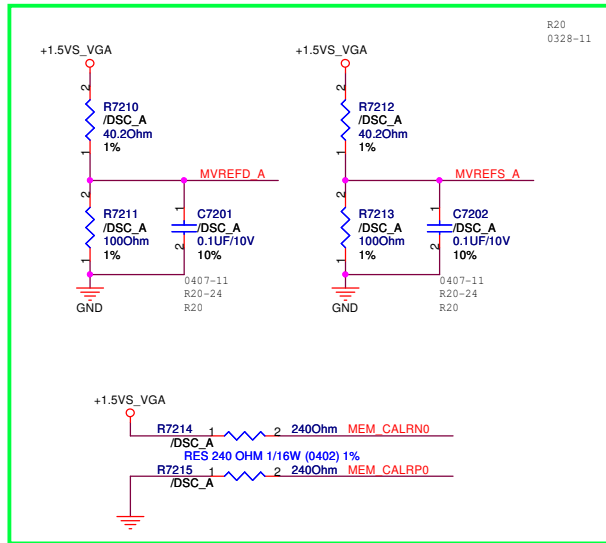
R 1.1 /0301 Seymour XT/M2



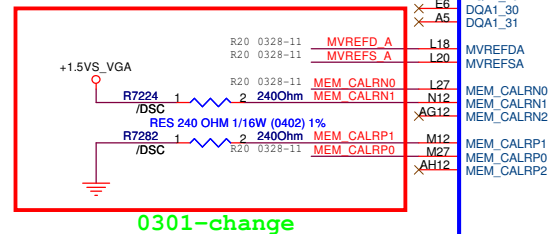


The all balls are NC except N12 /M12 for seymour

Reserve, Unmount



The all balls are NC except N12 /M12 for seymour



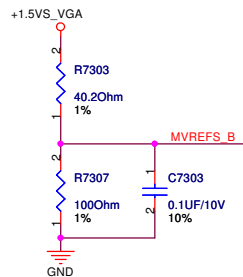
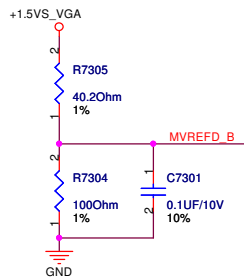
0301-change

U7001C 02V050000003

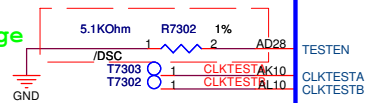
MEMORY INTERFACE A

MEMORY INTERFACE A		MEMORY INTERFACE B	
C37	DQAO_0	MAA0_0	G24
C35	DQAO_1	MAA0_1	J23
A35	DQAO_2	MAA0_2	H24
E32	DQAO_3	MAA0_3	J24
D33	DQAO_4	MAA0_4	J25
F32	DQAO_5	MAA0_5	H21
E32	DQAO_6	MAA0_6	G21
D31	DQAO_7	MAA0_7	H19
F30	DQAO_8	MAA1_0	H20
A30	DQAO_9	MAA1_1	G13
F28	DQAO_10	MAA1_2	G16
C28	DQAO_11	MAA1_3	H16
A28	DQAO_12	MAA1_4	J17
E28	DQAO_13	MAA1_5	H17
D27	DQAO_14	MAA1_6	A32
C26	DQAO_15	MAA1_7	C32
F26	DQAO_16	WCKA0_0	D23
A26	DQAO_17	WCKA0B_0	E22
F24	DQAO_18	WCKA0B_1	C14
C24	DQAO_19	WCKA1_0	A14
A24	DQAO_20	WCKA1B_0	F9
E24	DQAO_21	WCKA1_1	C34
C22	DQAO_22	WCKA1B_1	D29
A22	DQAO_23	EDCA0_0	D25
F22	DQAO_24	EDCA0_1	E16
D21	DQAO_25	EDCA0_2	E12
A20	DQAO_26	EDCA1_0	E12
F20	DQAO_27	EDCA1_1	EDCA1_2
D19	DQAO_28	EDCA1_3	A34
E18	DQAO_29	EDCA1_3	E28
C18	DQAO_30	EDCA1_3	C20
A18	DQAO_31	EDCA1_3	C16
F18	DQAO_0	EDCA1_3	C12
D17	DQAO_1	EDCA1_3	J11
E16	DQAO_2	EDCA1_3	F8
D15	DQAO_3	EDCA1_3	J21
F14	DQAO_4	EDCA1_3	G19
E14	DQAO_5	EDCA1_3	H27
D13	DQAO_6	EDCA1_3	G27
F12	DQAO_7	EDCA1_3	J14
A12	DQAO_8	EDCA1_3	H14
E11	DQAO_9	EDCA1_3	K23
D10	DQAO_10	EDCA1_3	K19
F10	DQAO_11	EDCA1_3	K20
A10	DQAO_12	EDCA1_3	K17
C10	DQAO_13	EDCA1_3	K24
E10	DQAO_14	EDCA1_3	K27
D9	DQAO_15	EDCA1_3	M13
F9	DQAO_16	EDCA1_3	K16
C9	DQAO_17	EDCA1_3	K26
A9	DQAO_18	EDCA1_3	J15
E9	DQAO_19	EDCA1_3	
D8	DQAO_20	EDCA1_3	
F8	DQAO_21	EDCA1_3	
A8	DQAO_22	EDCA1_3	
E8	DQAO_23	EDCA1_3	
D7	DQAO_24	EDCA1_3	
F7	DQAO_25	EDCA1_3	
C7	DQAO_26	EDCA1_3	
A7	DQAO_27	EDCA1_3	
E7	DQAO_28	EDCA1_3	
D6	DQAO_29	EDCA1_3	
F6	DQAO_30	EDCA1_3	
C6	DQAO_31	EDCA1_3	
A6	DQAO_32	EDCA1_3	
E6	DQAO_33	EDCA1_3	
D5	DQAO_34	EDCA1_3	
F5	DQAO_35	EDCA1_3	
C5	DQAO_36	EDCA1_3	
A5	DQAO_37	EDCA1_3	
E5	DQAO_38	EDCA1_3	
D4	DQAO_39	EDCA1_3	
F4	DQAO_40	EDCA1_3	
C4	DQAO_41	EDCA1_3	
A4	DQAO_42	EDCA1_3	
E4	DQAO_43	EDCA1_3	
D3	DQAO_44	EDCA1_3	
F3	DQAO_45	EDCA1_3	
C3	DQAO_46	EDCA1_3	
A3	DQAO_47	EDCA1_3	
E3	DQAO_48	EDCA1_3	
D2	DQAO_49	EDCA1_3	
F2	DQAO_50	EDCA1_3	
C2	DQAO_51	EDCA1_3	
A2	DQAO_52	EDCA1_3	
E2	DQAO_53	EDCA1_3	
D1	DQAO_54	EDCA1_3	
F1	DQAO_55	EDCA1_3	
C1	DQAO_56	EDCA1_3	
A1	DQAO_57	EDCA1_3	
E1	DQAO_58	EDCA1_3	
D0	DQAO_59	EDCA1_3	
F0	DQAO_60	EDCA1_3	
C0	DQAO_61	EDCA1_3	

PRO-M2



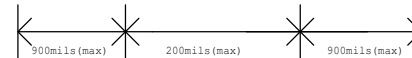
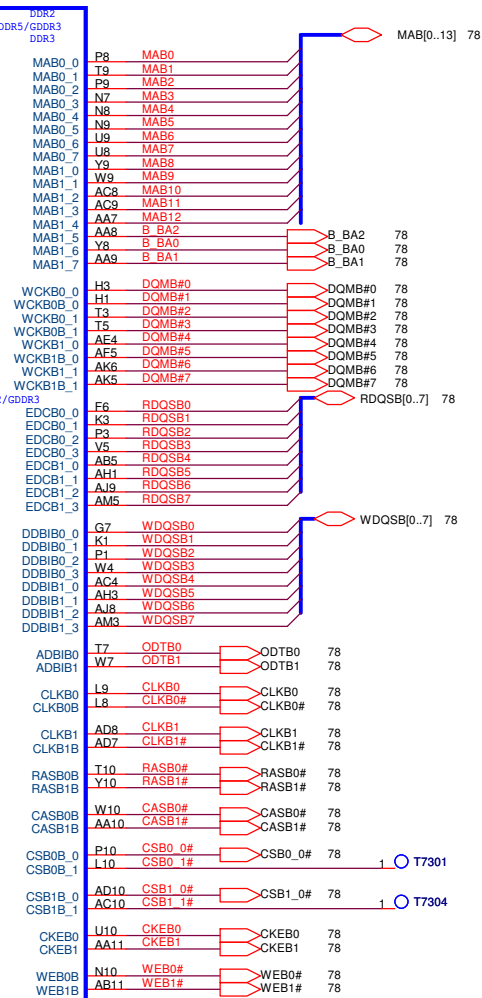
0301-change



U7001D 02V050000003

MEMORY INTERFACE B

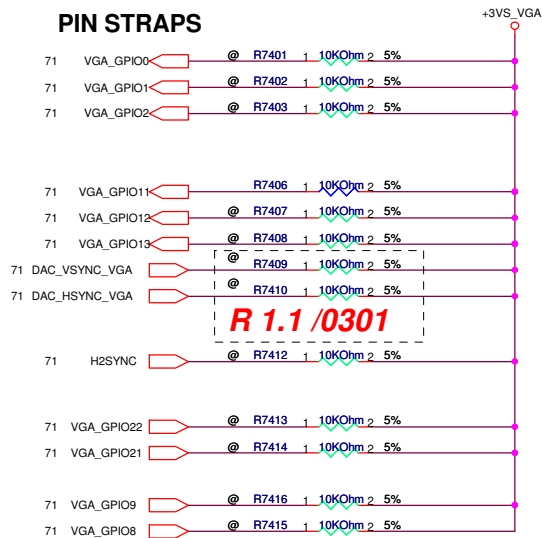
PRO-M2



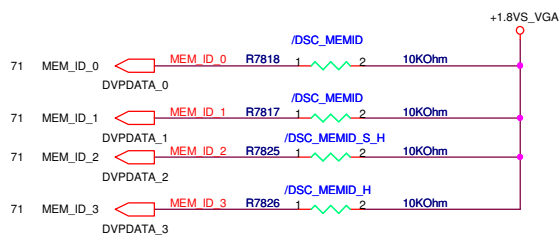
follow up checklist suggestion 0301-change

GPIO21 MUST BE LOW DURING PERSTB WHEN BEING USED TO CONTROL MVDDQ

PIN STRAPS



VRAM size define by VBIOS



+1.8VS_VGA 57,71,75,76,91
 +3VS_VGA 57,70,71,75,91

Seymour Straps

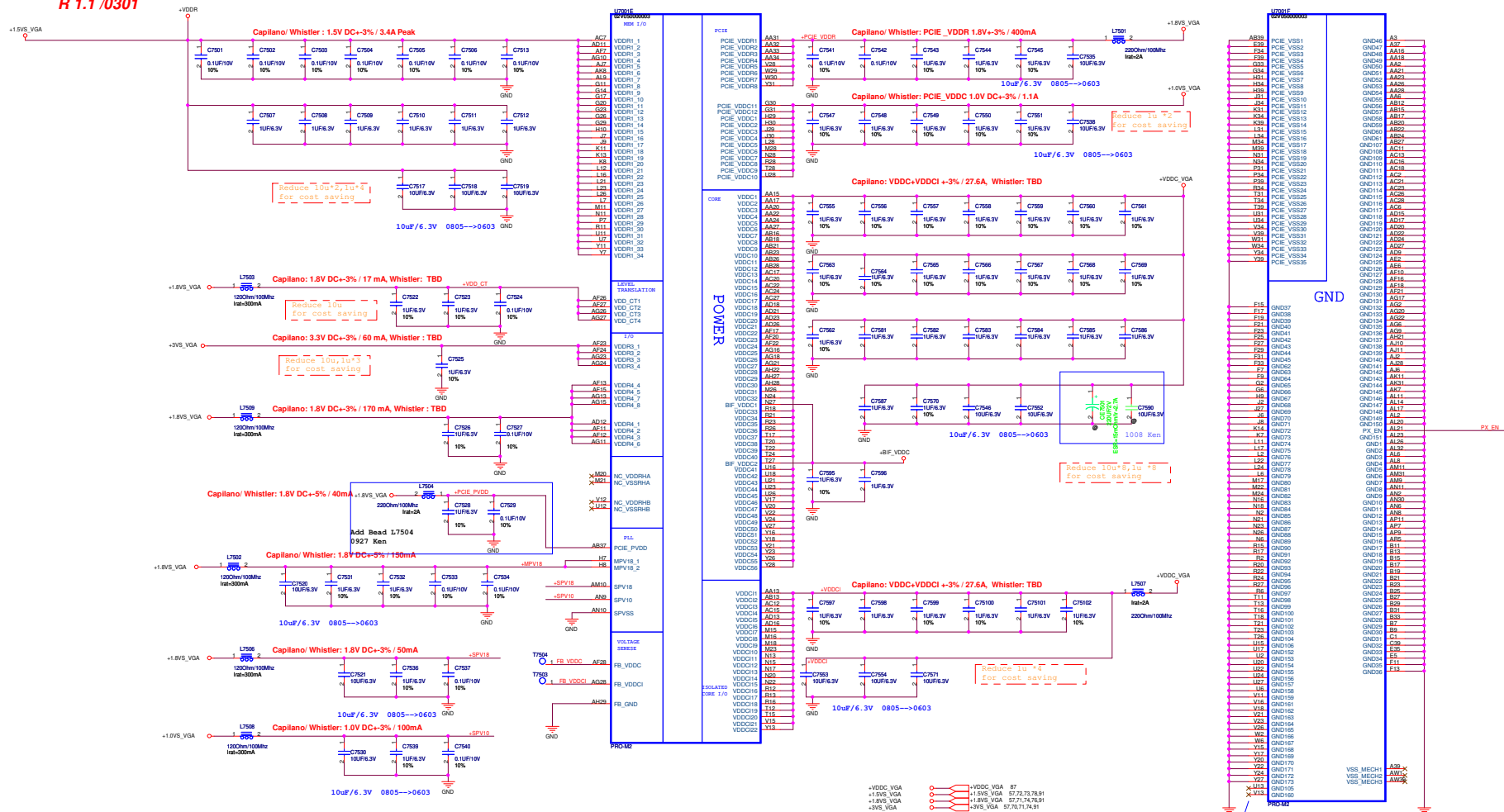
STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing This setting can only be used if the PCIE bus design meets the "Low Loss interconnect" requirements.	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled MXM and add-in boards	0 (internal pull-down)
BIF_GEN2_EN_A	GPIO2	1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on 0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on	0
VGA_DIS	GPIO9	0 - VGA Controller capacity enabled 1 - The device will not be recognized as the system's VGA controller	0 (internal pull-down)
ROMIDCFG(2:0)	GPIO(13:11)	If BIOS_ROM_EN=1, then Config[2:0] defines the ROM type. If BIOS_ROM_EN=0, then Config[2:0] defines the primary memory aperture size. 128MB---000 32MB---Not Support 2GB---Not Support 256MB---001 512MB---Not Support 4GB---Not Support 64MB---010 1GB---Not Support	0000 (internal pull-down)
BIOS_ROM_EN	GPIO22_ROMCSB	Enable external BIOS ROM device 0-Disable external BIOS ROM device 1-Enable external BIOS ROM device	0 (internal pull-down)
AUD[1:0] AUD[0]	HSYNC VSYNC	AUD[1:0]: 00: No audio function; 01: Audio for DisplayPort and HDMI if adapter is detected; 10: Audio for DisplayPort only; 11: Audio for both DisplayPort and HDMI.	0 (internal pull-down)
Reserved	GENLK_CLK GPIO_21_BB_EN GPIO8	ATI internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET.	0 (internal pull-down)

Seymour XT:

Memory ID Board Straps

Vendor	DVPDATA(3,2,1,0)	ID	DDR3 Memory Type	VRAM Vendor Part
Hynix	0000	0	64M*16*4 pcs(512MB)	H5TO1G63BFR-12 (1600Mbps)
	0001	1	64M*16*4 pcs(512MB)	H5TO1G63BFR-12C (1600Mbps)
	0010	2	128M*16*4 pcs(1GB)	H5TQ2G63BFR-12C (1600Mbps)
	0011	3	128M*16*4 pcs(1GB)	H5TQ2G63BFR-11C LF (1800Mbps)
	0100	4		
	0101	5		
	0110	6		
	0111	7		
Samsung	1000	8	64M*16*4 pcs(512MB)	K4W1G1646E-HC12 (1600Mbps)
	1001	9	64M*16*4 pcs(512MB)	K4W1G1646G-BC12 (1600Mbps)
	1010	10	128M*16*4 pcs(1GB)	K4W2G1646B-HC12 (1600Mbps)
	1011	11	128M*16*4 pcs(1GB)	K4W2G1646C-HC12 (1600Mbps)
	1100	12		
	1101	13		
	1110	14		
	1111	15		

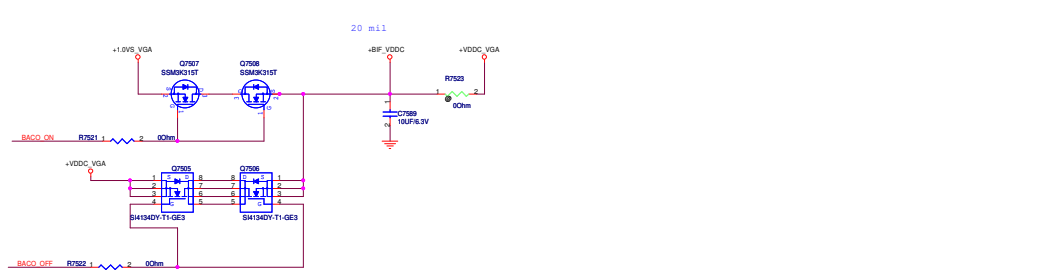
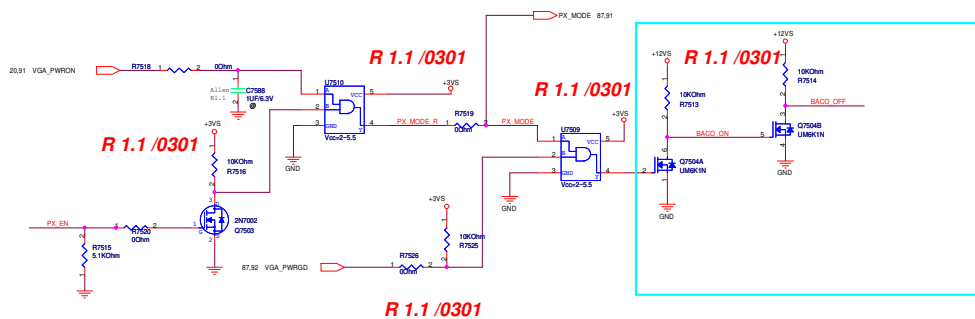
R 1.1 /0301



PX_EN=0: Normal Operation
PX_EN=1: BACO Mode

BIF short with +VDDC_VGA if BACO is not support
BIF_VDDC: I=55mA@BACO MODE (AN_MGEN_R5)

NC for seymour

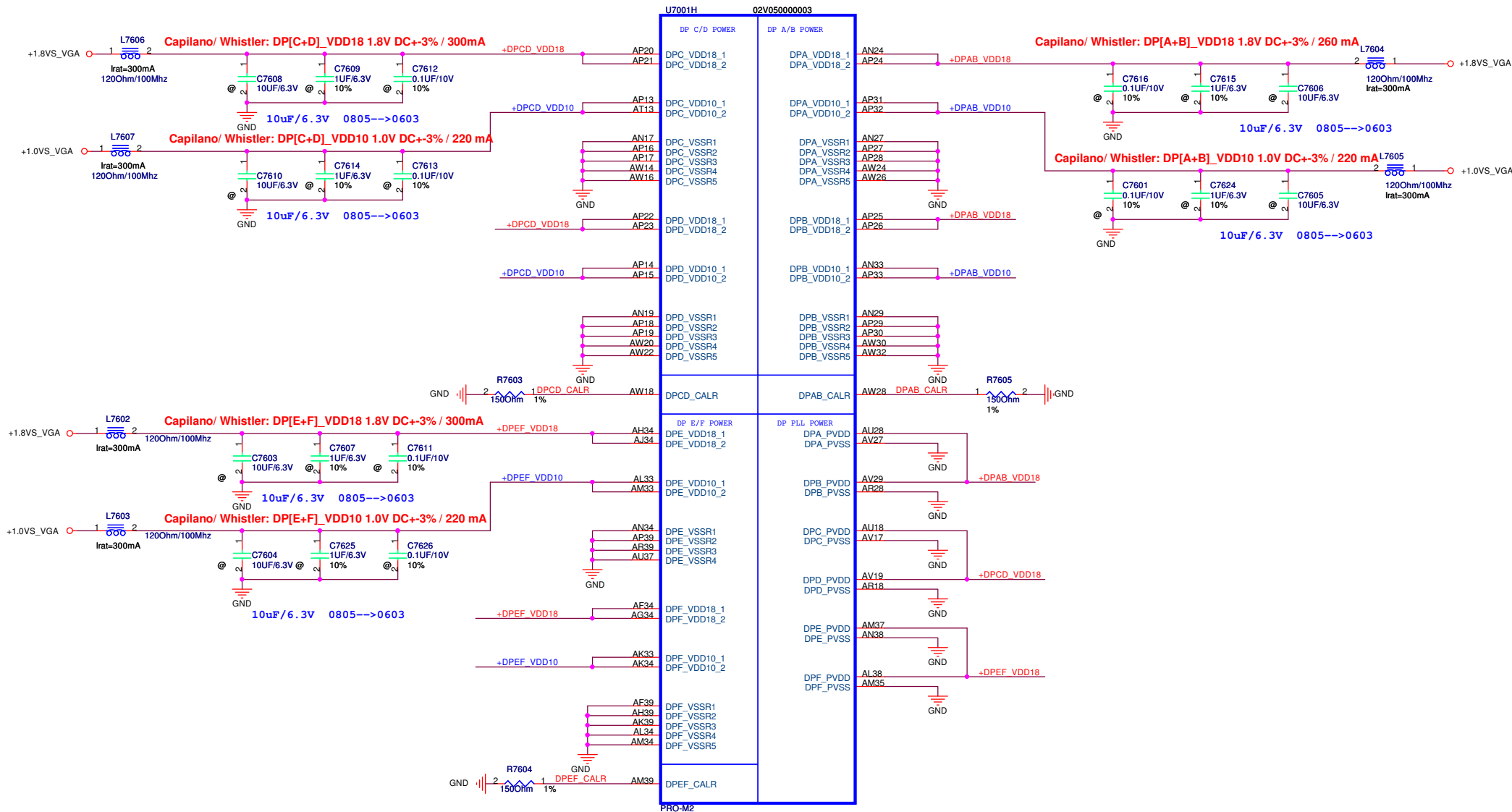


0301-change

PX with BACO mode all displays are always driven by APU
DPA&DPB share power ;DPC&DPD share power ;DPE&DPF share power

+1.0VS_VGA
+1.8VS_VGA

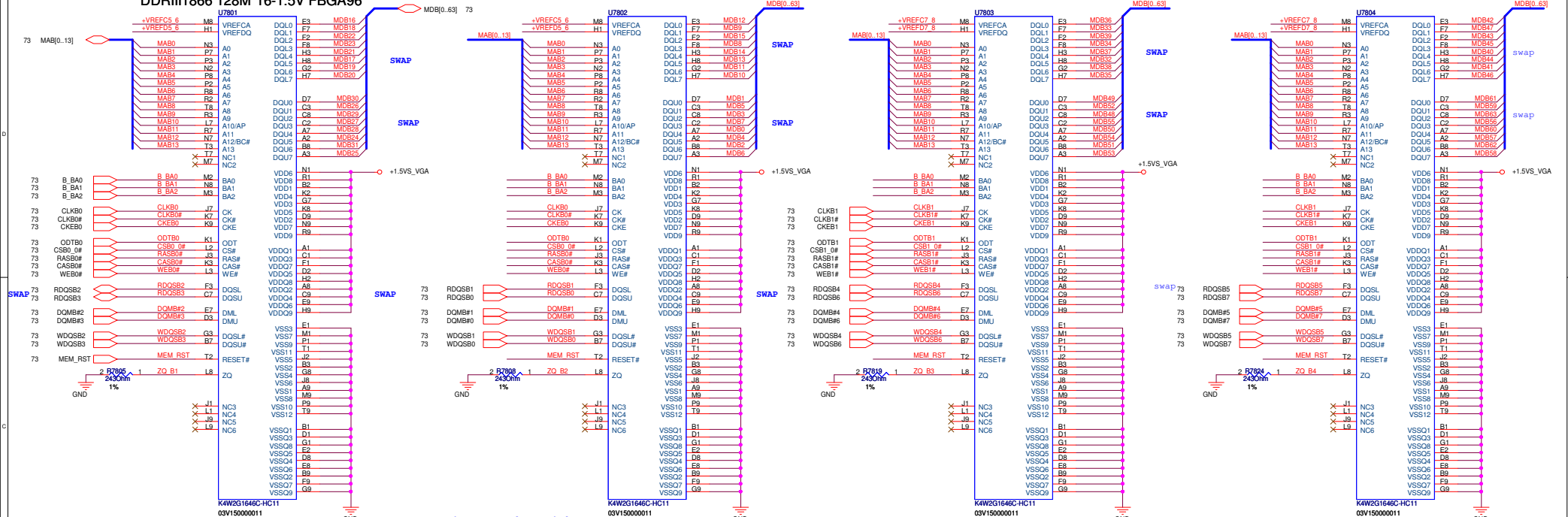
+1.0VS_VGA 57,70,71,75,91
+1.8VS_VGA 57,71,74,75,91



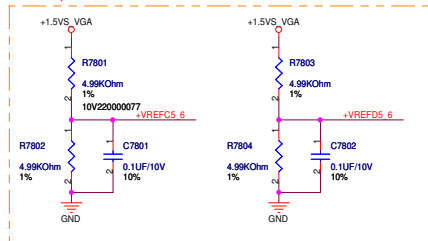


PEGATRON		Title : GPU-MEM CHA	
BG1/BU1		Engineer: Allen_CD_Wu	
Size	Project Name		Rev
C	AAB70		1.1
Date: Monday, March 21, 2011		Sheet	77 of 99

DDRIII1866 128M*16-1.5V FBGA96

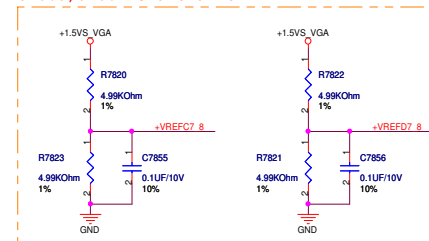


U7801,U7802 share a Verf



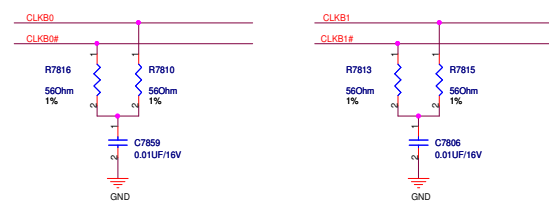
VRAM change to colay symbal
1.1_72 1110 Ken

cost saving

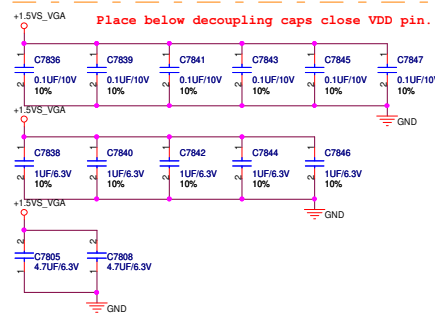


cost saving

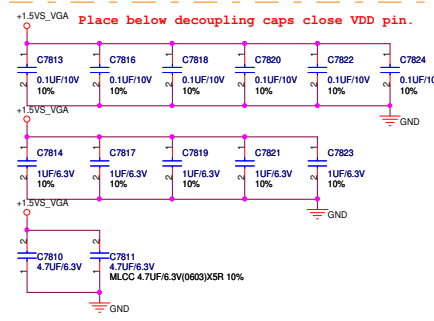
7.5uF per one VRAM



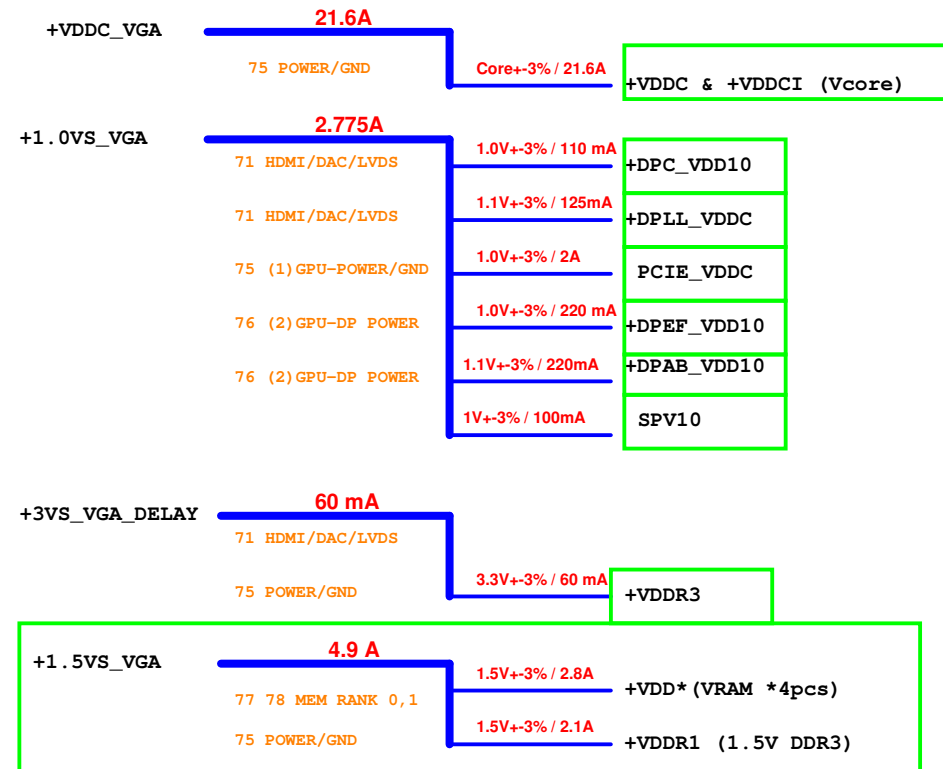
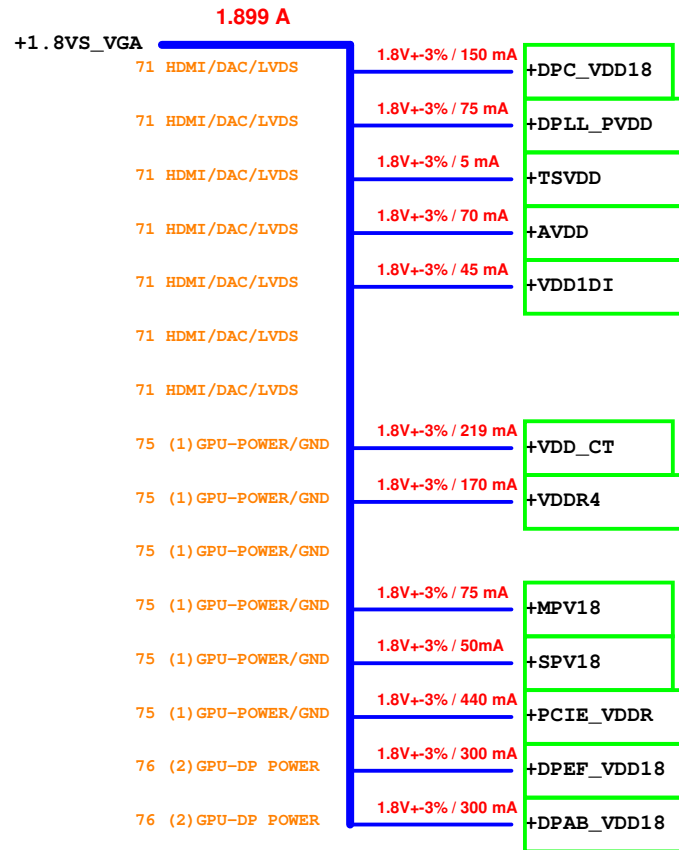
Place below decoupling caps close VDD pin.



GA Place below decoupling caps close VDD pin



+1.5VS_VGA +1.5VS_VGA 57,72,73,75,91



Total:15W (w/o VRAM)

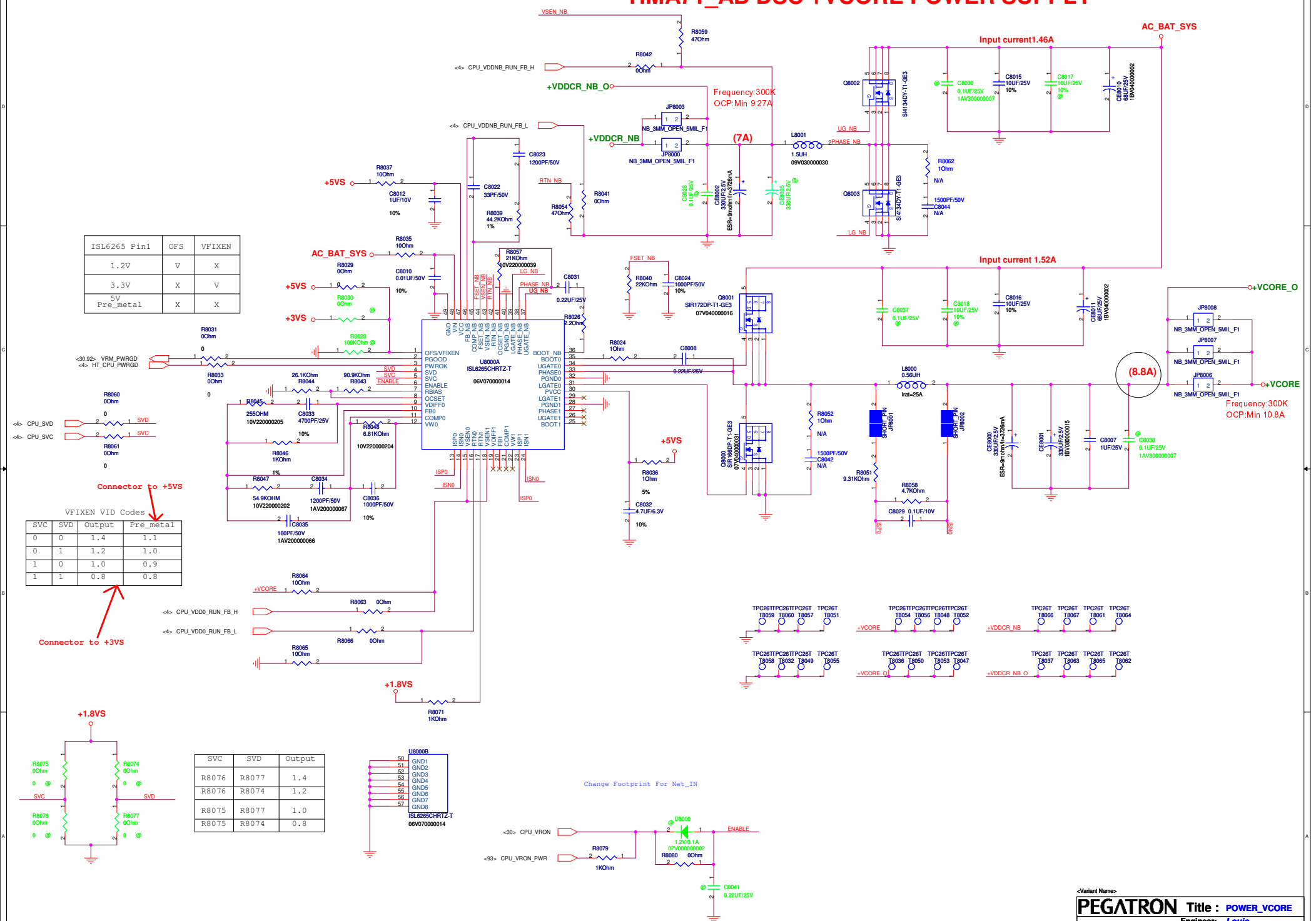
Power Up Sequence :

+VGA_VCORE -> +1.05VS_VGA -> +1.5VS_VGA -> +1.8VS_VGA -> +3VS_VGA_DELAY

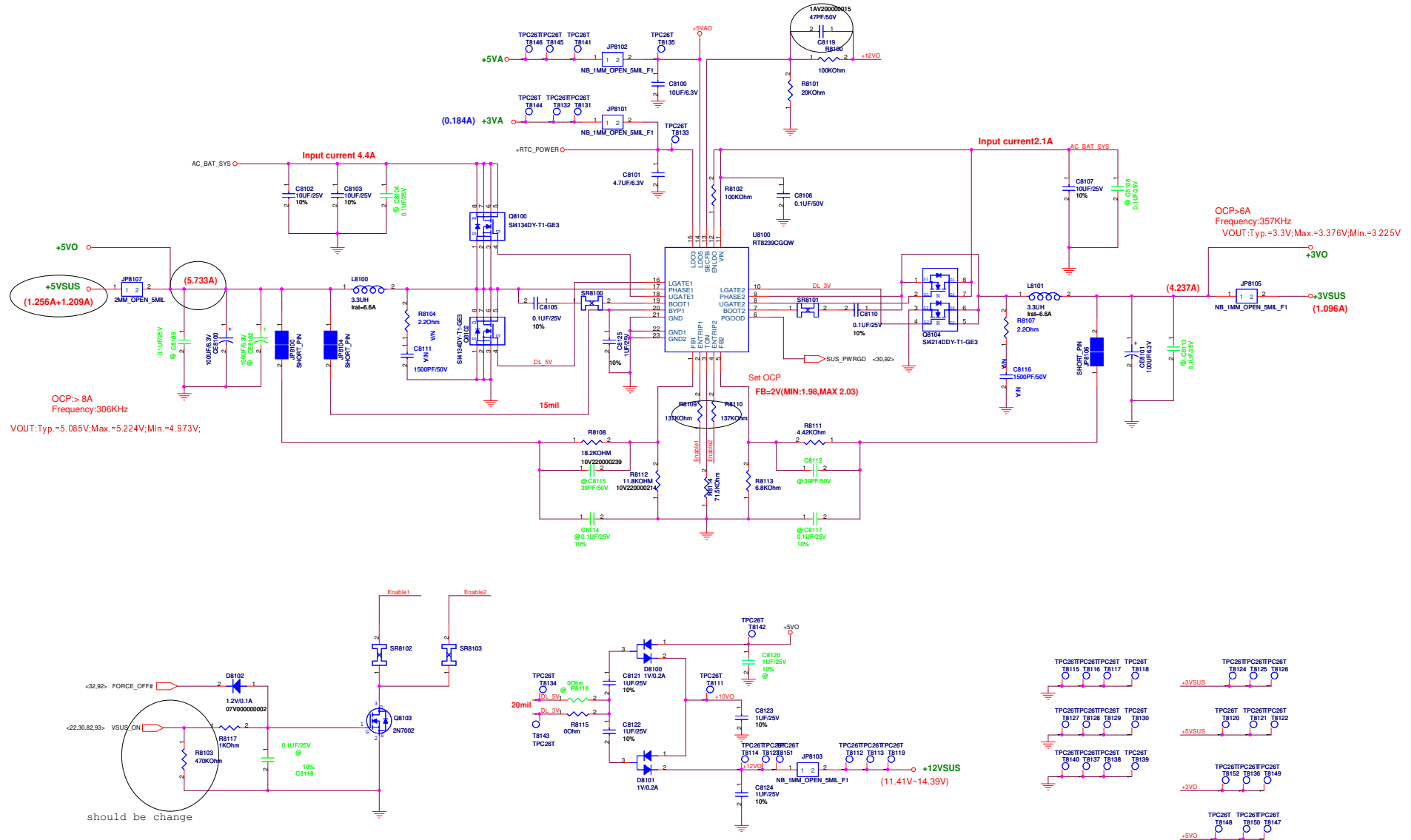
Power Down Sequence :

+3VS_VGA_DELAY -> +1.8VS_VGA -> +1.5VS_VGA -> +1.05VS_VGA -> +VGA_VCORE

HMA71_AB DSC +VCORE POWER SUPPLY



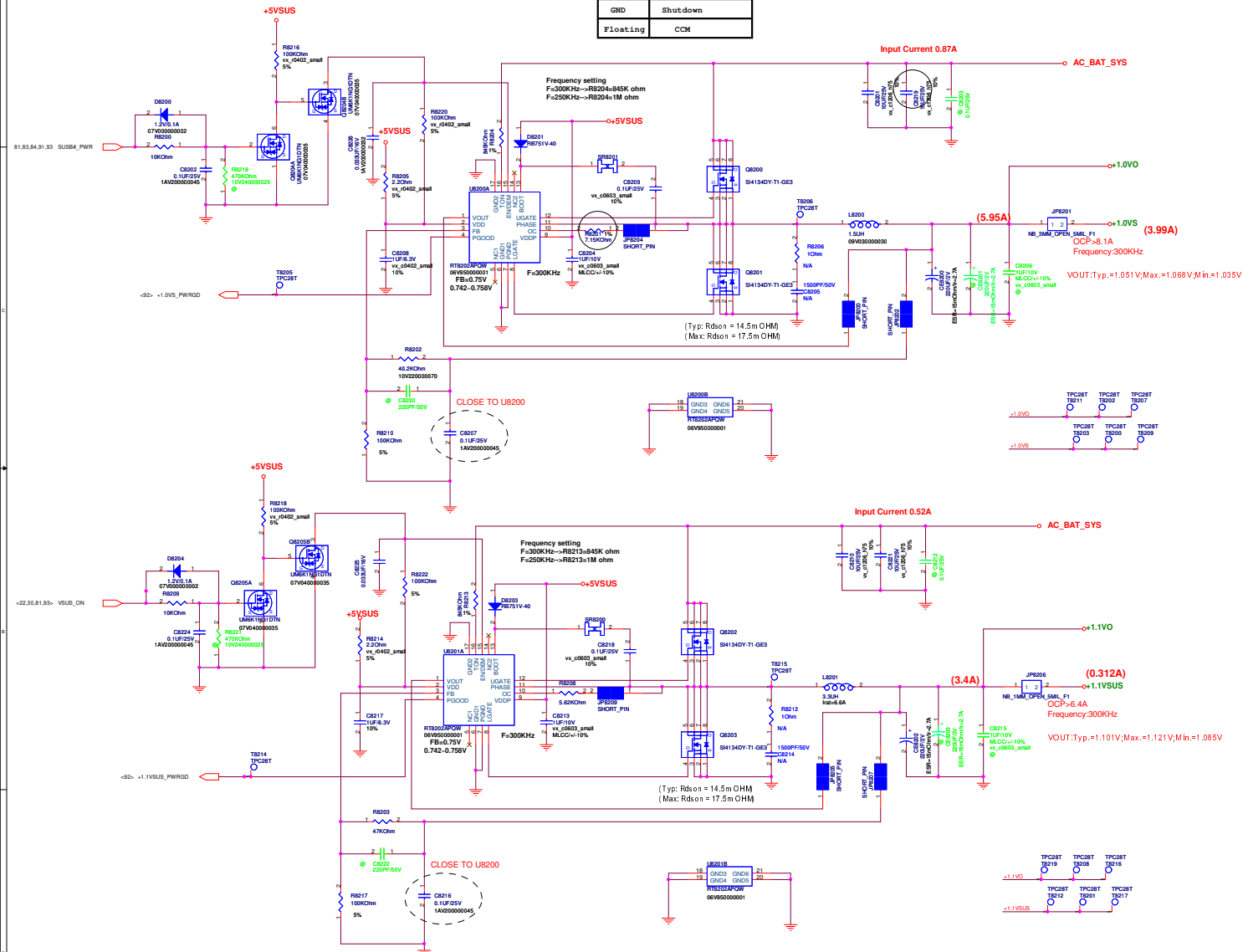
HMA71 DSC +SYSTEM POWER SUPPLY



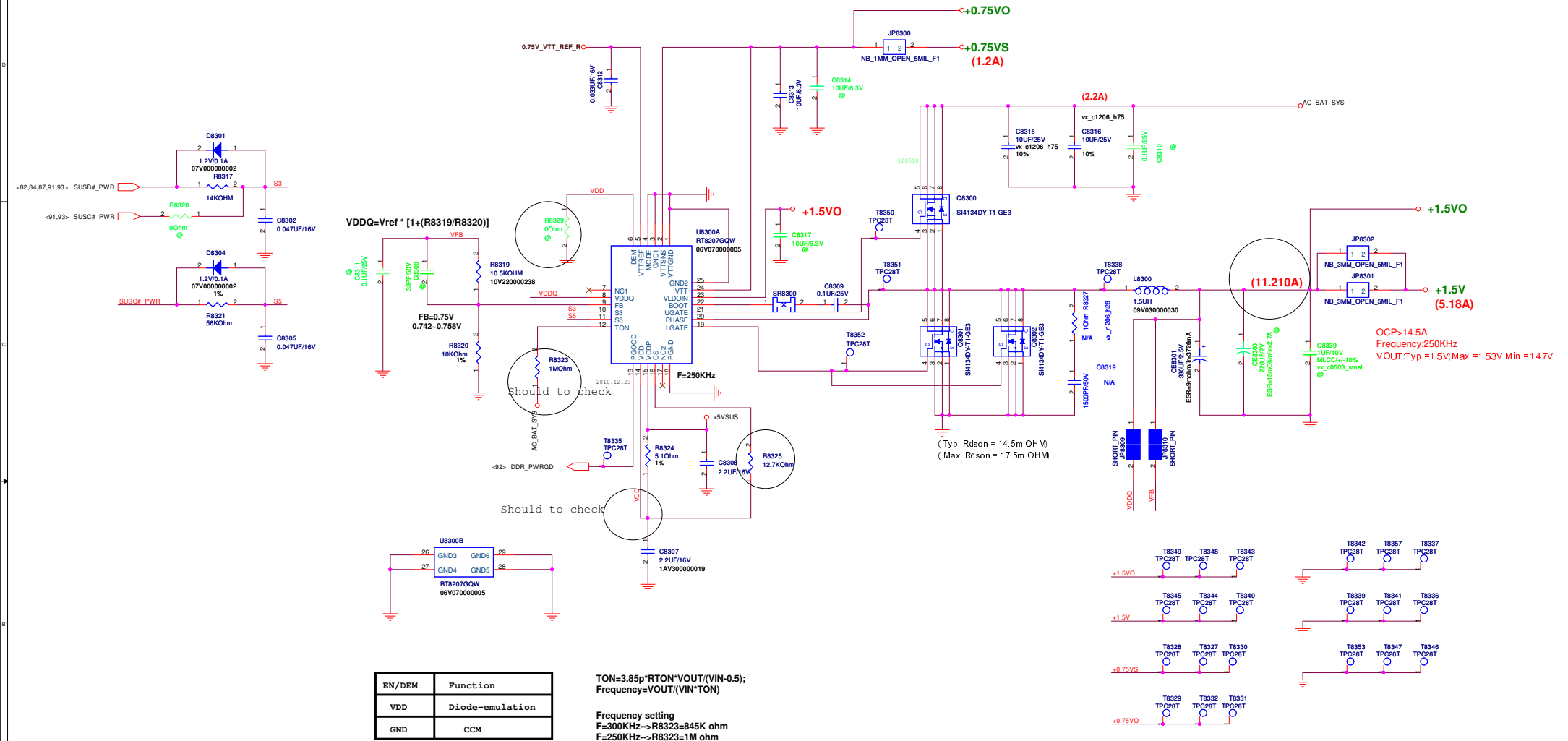
HMA71 DSC +1.0V0&+1.1V0 POWER SUPPLY

P.82

EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM



+1.5VO & +0.75VS POWER SUPPLY



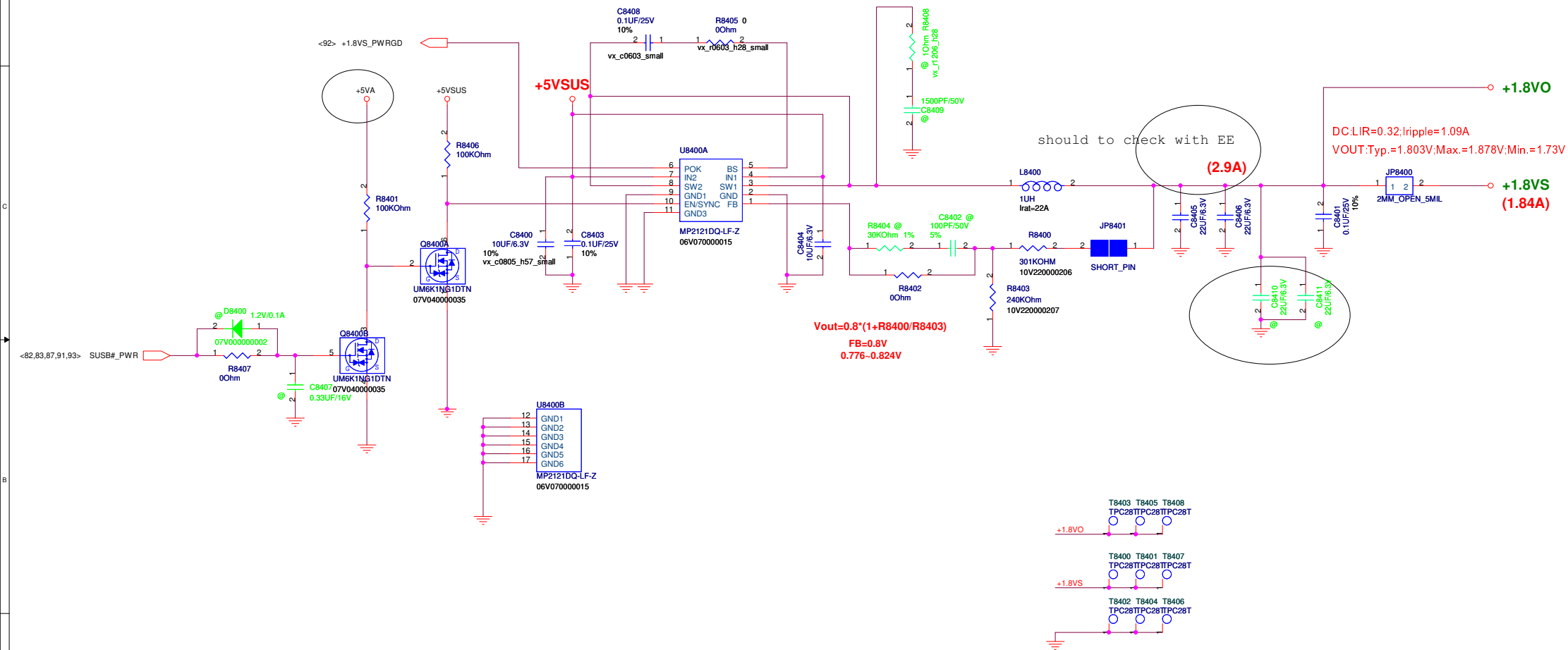
EN/DEM	Function
VDD	Diode-emulation
GND	CCM

$$\text{TON} = 3.85 \mu\text{s} \cdot \text{R}_{\text{TON}} \cdot \text{V}_{\text{OUT}} / (\text{V}_{\text{IN}} - 0.5);$$

$$\text{Frequency} = \text{V}_{\text{OUT}} / (\text{V}_{\text{IN}} \cdot \text{TON})$$

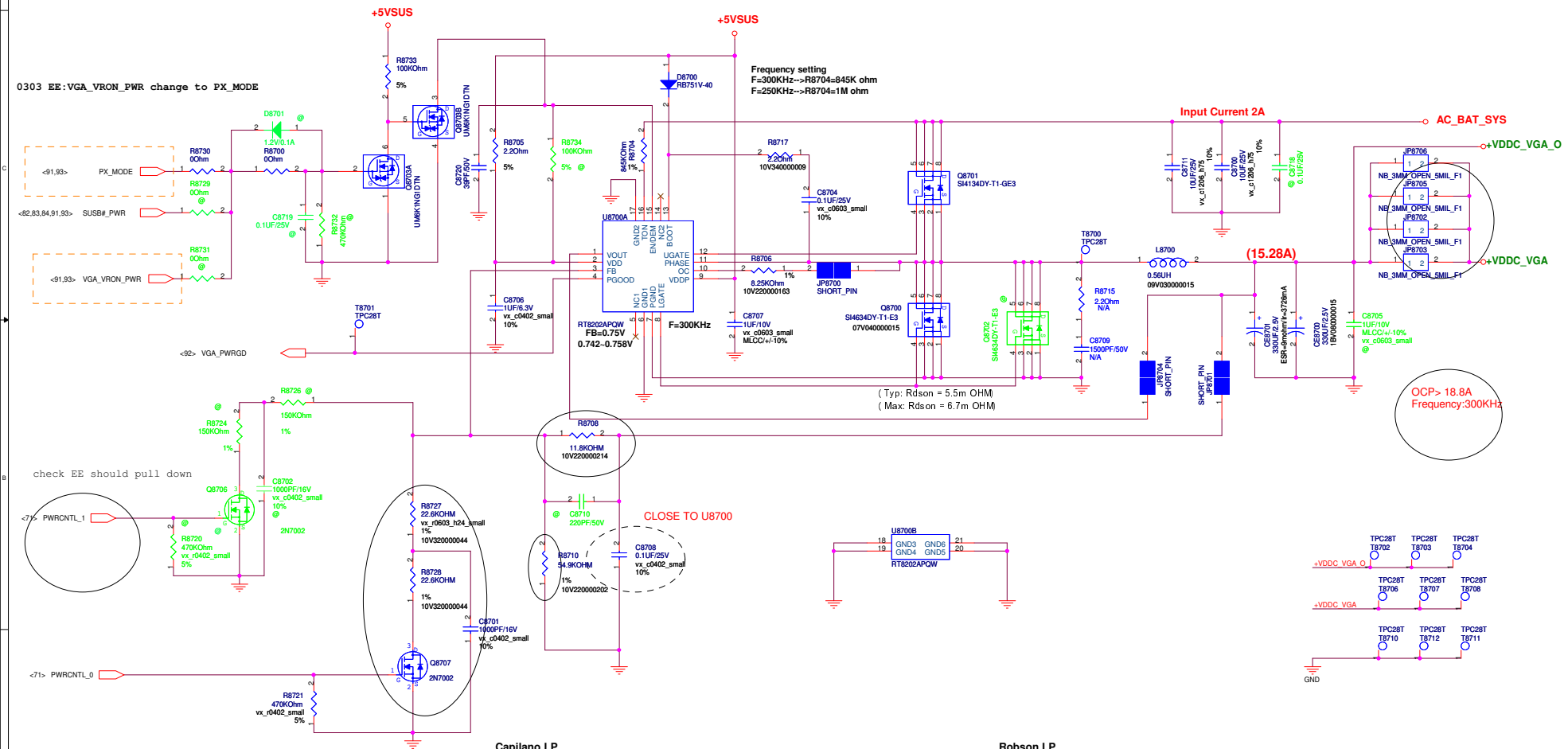
Frequency setting
F=300KHz-->R8323=845K ohm
F=250KHz-->R8323=1M ohm

+1.8VS POWER SUPPLY



AAB70 DSC +VGA_VCORE POWER SUPPLY

EN/DEM	Function
VDD	Diode-emulation
GND	Shutdown
Floating	CCM



Seymour XT (17W)

PWRCNTL_1 (GPIO20)	PWRCNTL_0 (GPIO15)	+VGA_VCORE
LOW	LOW	0.9V/real 0.911V
LOW	HIGH	1.1V / real1.107V

Capilano LP

PWRCNTL_1 (GPIO20)	PWRCNTL_0 (GPIO15)	+VGA_VCORE
LOW	LOW	1V
LOW	HIGH	0.9V
HIGH	HIGH	0.95V

R8727=75K ohm
R8728=75K ohm
R8726, R8724, R8720, Q8708 must be mounted.

Robson LP

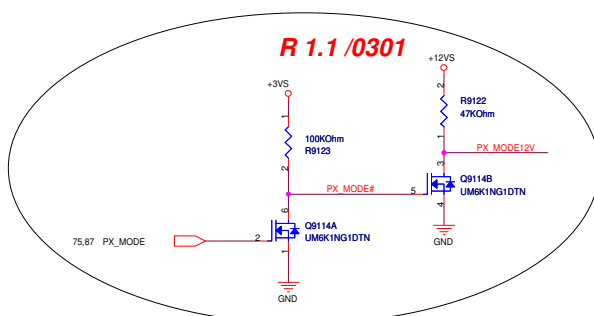
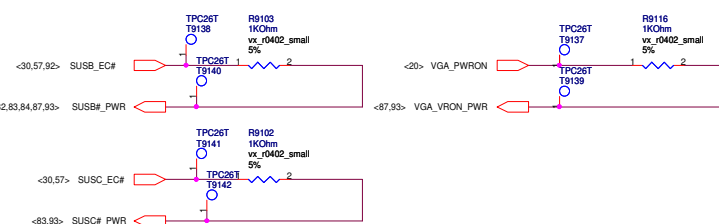
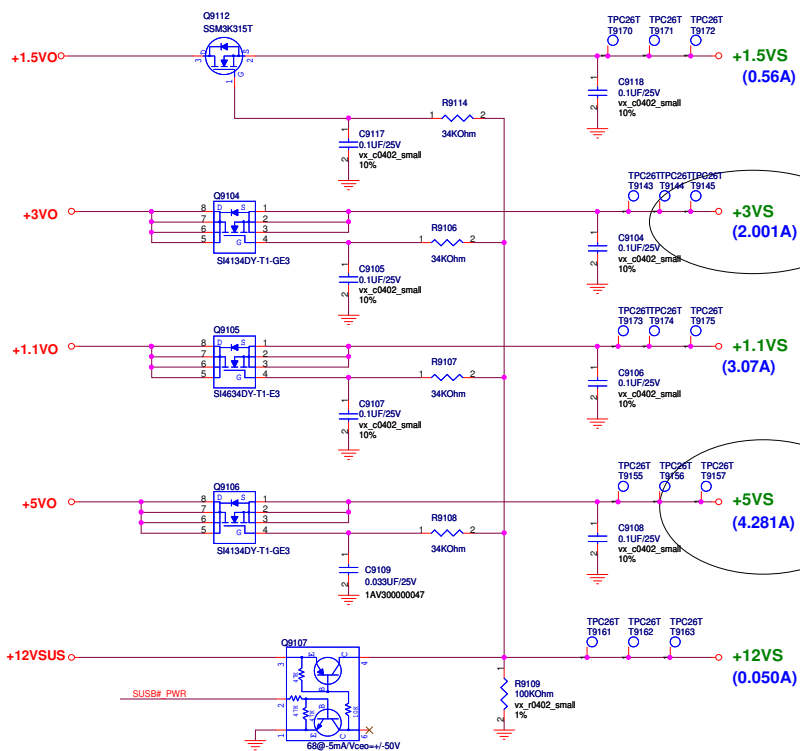
PWRCNTL_1 (GPIO20)	PWRCNTL_0 (GPIO15)	+VGA_VCORR
LOW	LOW	0.95V
LOW	HIGH	0.9V

BATTERY IN DETECT

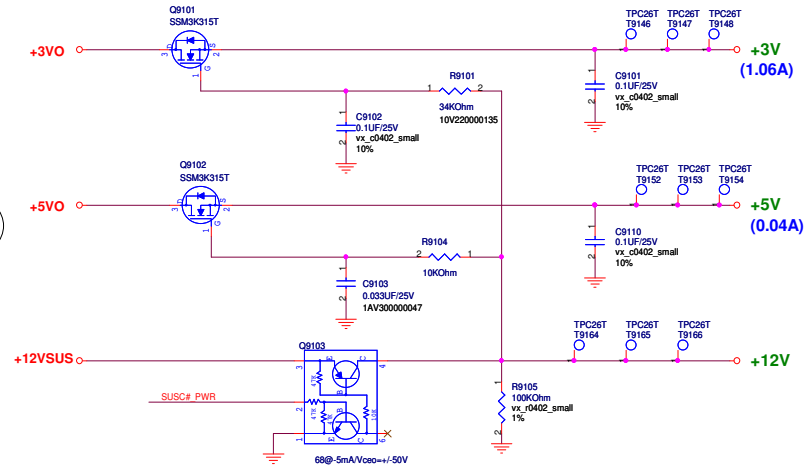


<Variant Name>			
PEGATRON		Title :POWER_DETECT	
		Engineer: <i>Louis</i>	
Size	Project Name		Rev
Custom			1.0
Date: <i>Wednesday, May 04, 2011</i>		Sheet	90 of 99

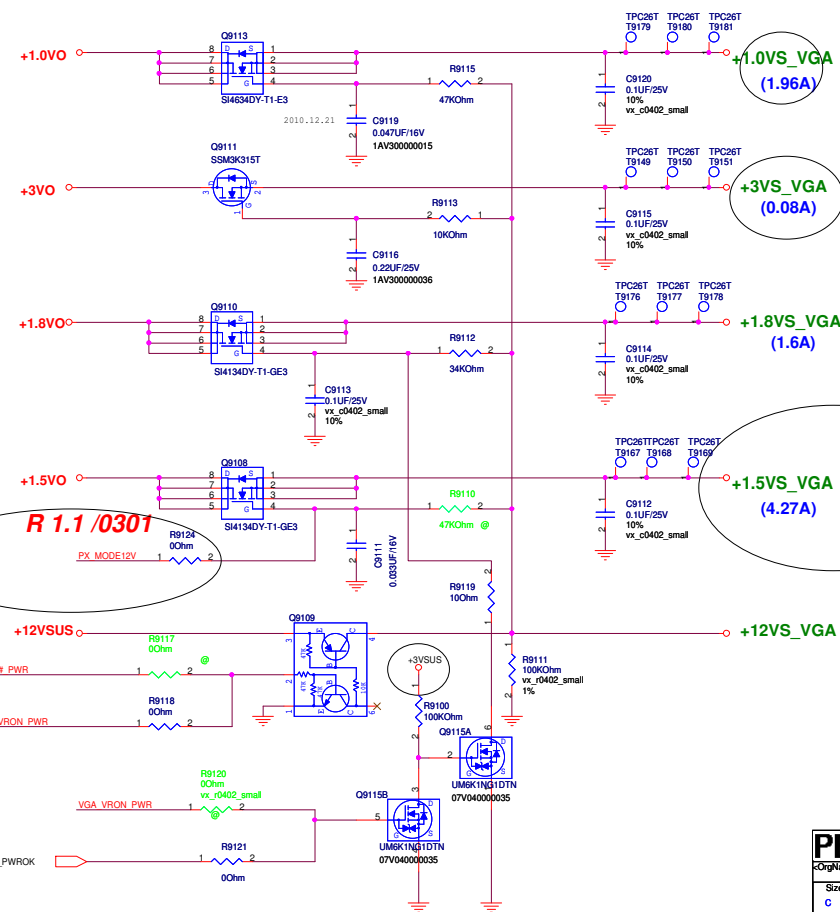
SUSB#_PWR POWER



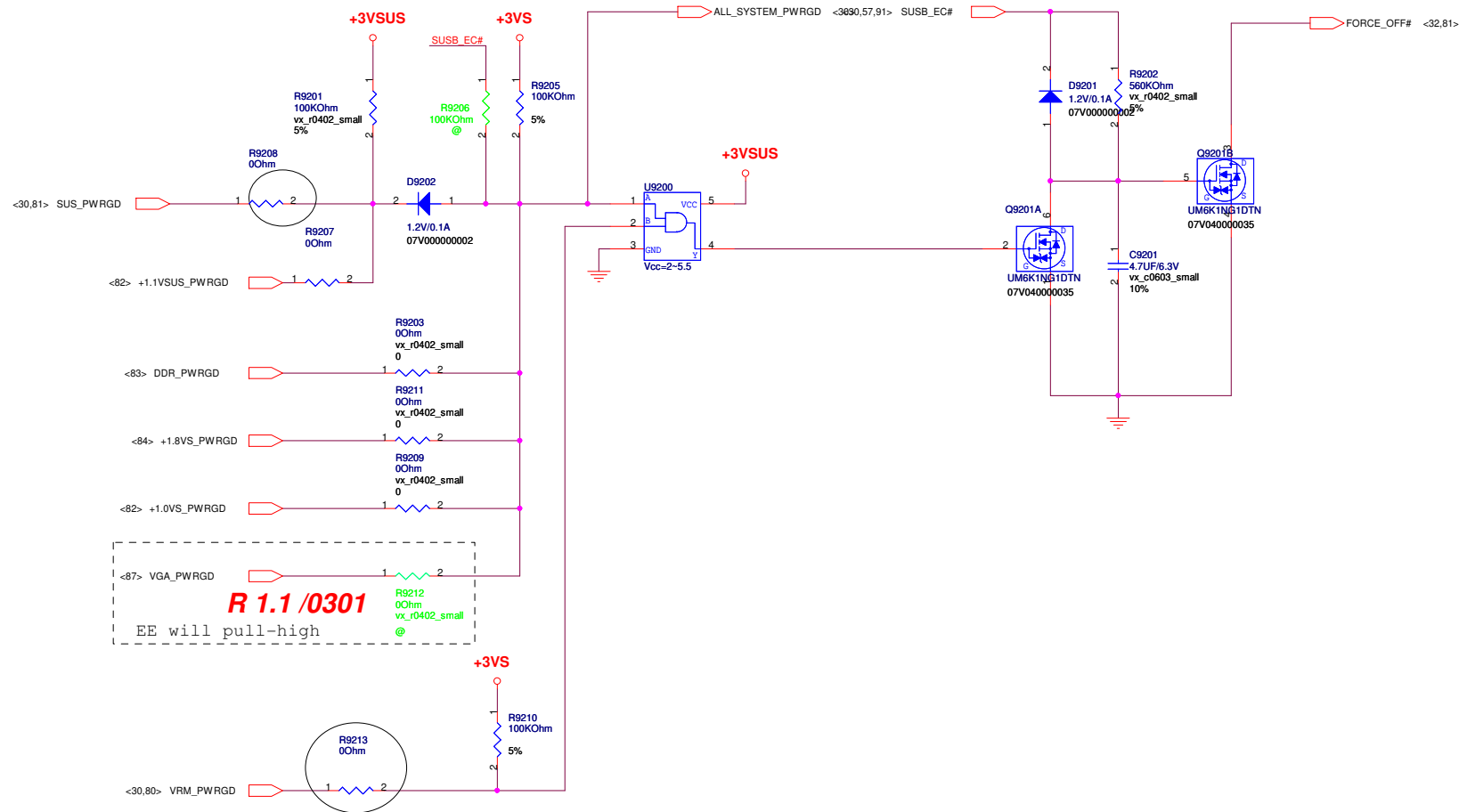
SUSC#_PWR POWER

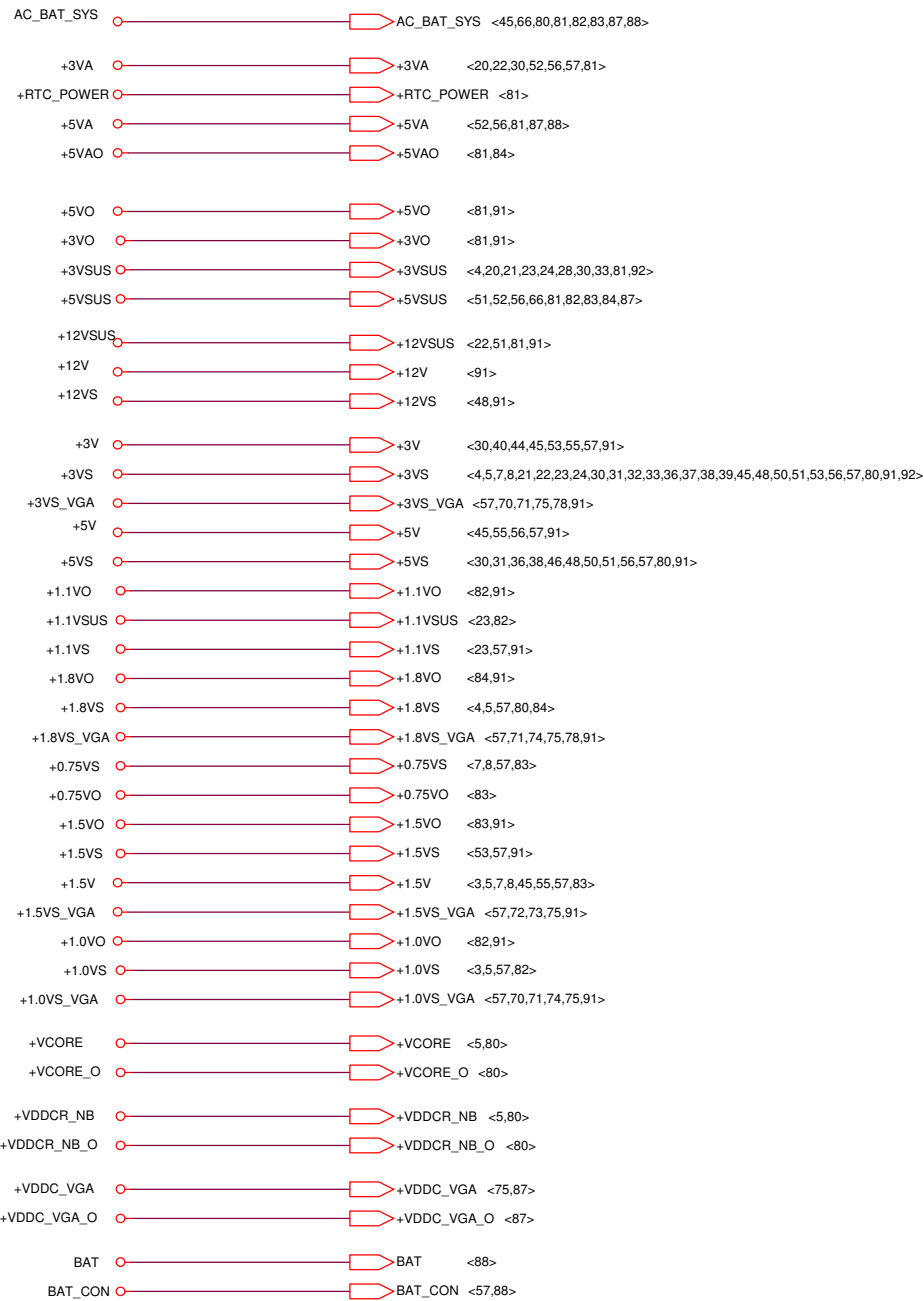


VGA_VRON_PWR_PWR POWER

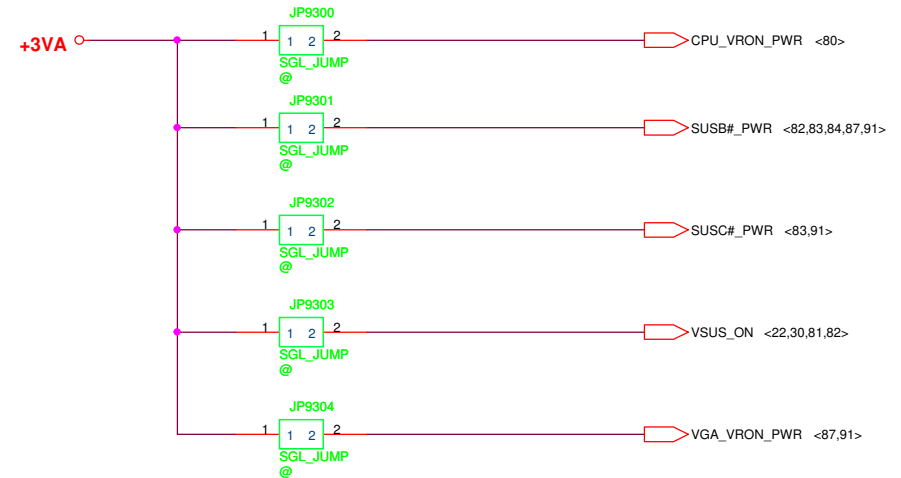


POWER GOOD DETECTOR





FOR POWER TEST



<Variant Name>		
PEGATRON Title :POWER_SIGNAL		
Engineer: Louis		
Size B	Project Name	Rev 1.0
Date: Wednesday, May 04, 2011 Sheet 93 of 99		

R20

Item	Date	Description
1	0328-11	P.72 Add R7210~R7215, C7201, C7202 for VRAM Channel A reseved. P.5 Change C0508=>0805, L0501=>1K 0603 for CRT ripple noise. P.39 Add R3909, R3910, R3914, R3915 for POP issue P.50 Add R5010, C5020, C5021, Q5001, U5005 for Thermal Palm rest. P.04 Add SP0410, SP0411 for Thermal Palm rest. P.32 Add R3210 for Thermal Palm rest.
7	0330-11	P.98 Copy TP BTN Board from AIH24
8		P.66 Add 2nd USB power switch (U6605) for Audio board USB port voltage drop
9		P.50 Un-mount R5010, C5020, C5021, Q5001, U5005
10	0331-11	P.22 Add Test Pad T2201, T2202 for U2001.W5 and AE29 ICT function.
11		P38. Update CON3801, CON3802=>1217-00P1000
12		P66. Update CON6602=>1218-01BJ000
13		P99. Update IOCON5=>1218-01BJ000
14		P31. CON3102, CON3103=>1218-00C7000
15	0404-11	P65. Change H6539, H6541, H6542, H6545, H6633 to NPTH
16		P66. Change CON6603, CON6605 to 4 pin. Del C6605, C6608. Un-mount R6609
17		P97. Change PWR_U01 to 4 pin, delete PWR_R2, PWR_LED2
18	0406-11	P65. Modify H6541, H6542, H6545 GND
19		P33. Add L3303 for AVDDL EMI issue
20		P34. Add U3405 for EMI Home issue
21	0407-11	P66. Add CON6608
22		P99. Add IOCON6
23		P34. Un-mount R3408, R3409
24		P72. Un-mount C7201, C7202
25	0410-11	P39. R3905, R3906=> 51 ohm
26		P33. Mount R3317=> 10K
27		P46. Change L4601~L4603=> 56nH (Not yet)
28		P66. Change U6601=>1.5A, Mount U6605
29	0411-11	P30. Change R3035 option as /SJV_ID
30		P21. Change R3042 option as /SJV_ID
31	0421-11	P66. Change U6601, U6605 => 2.5A
32		P50. Change R5001 => 39K ohm for Thermal
33		P56. Change R5603,R5621 => 100 ohm,390 ohm ; LED5610,R5611=> 0713-1QJ000,0713-1QK000
34		P33. Change C3321,C3322 => 15PF
35		P33. Change L3303 => 0 ohm (0603)
36		P46. Change L4601, L4602, L4603 => 56nH for EMI
37		Update Power AAB7A_BRAZO_PWR_2R0_0411_DSC_A& AIC70 Sub board AIC70_R20_201104211100
38	0503-11	P66 unmount con6608
39	0504-11	P34 Mount R3408
40		P65 Un-mount H6535, H6536
41		P99 Un-mount IOCON6
42		Update Power AAB7A_BRAZO_PWR_2R0_0504_DSC_A
43	0505-11	P39 Un-mount R3910, Mount R3914=1M ohm

PEGATRON

Title :History

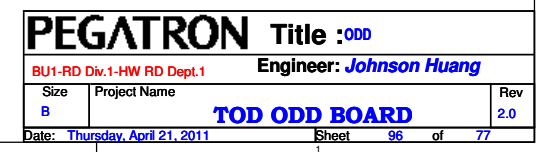
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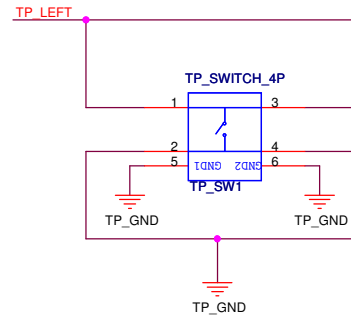
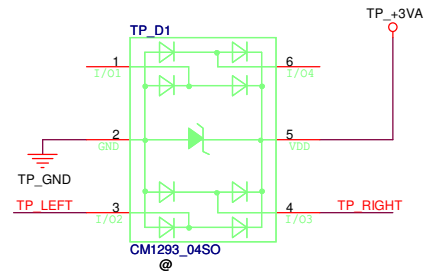
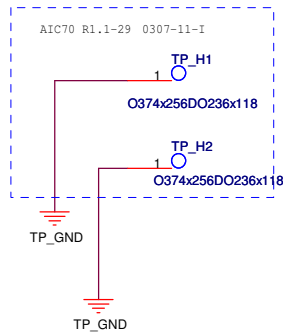
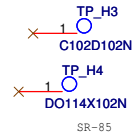
Size
B

Project Name
AAB70

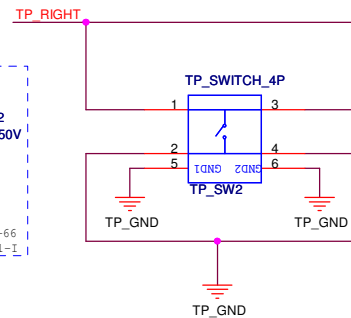
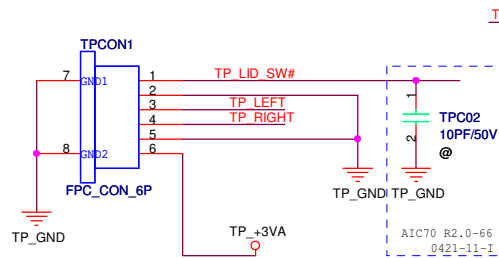
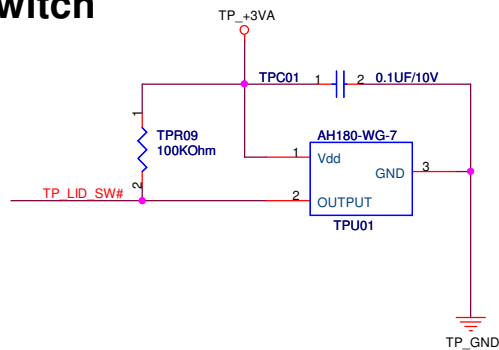
Rev
1.1

Date: Thursday, May 05, 2011Sheet 95 of 99



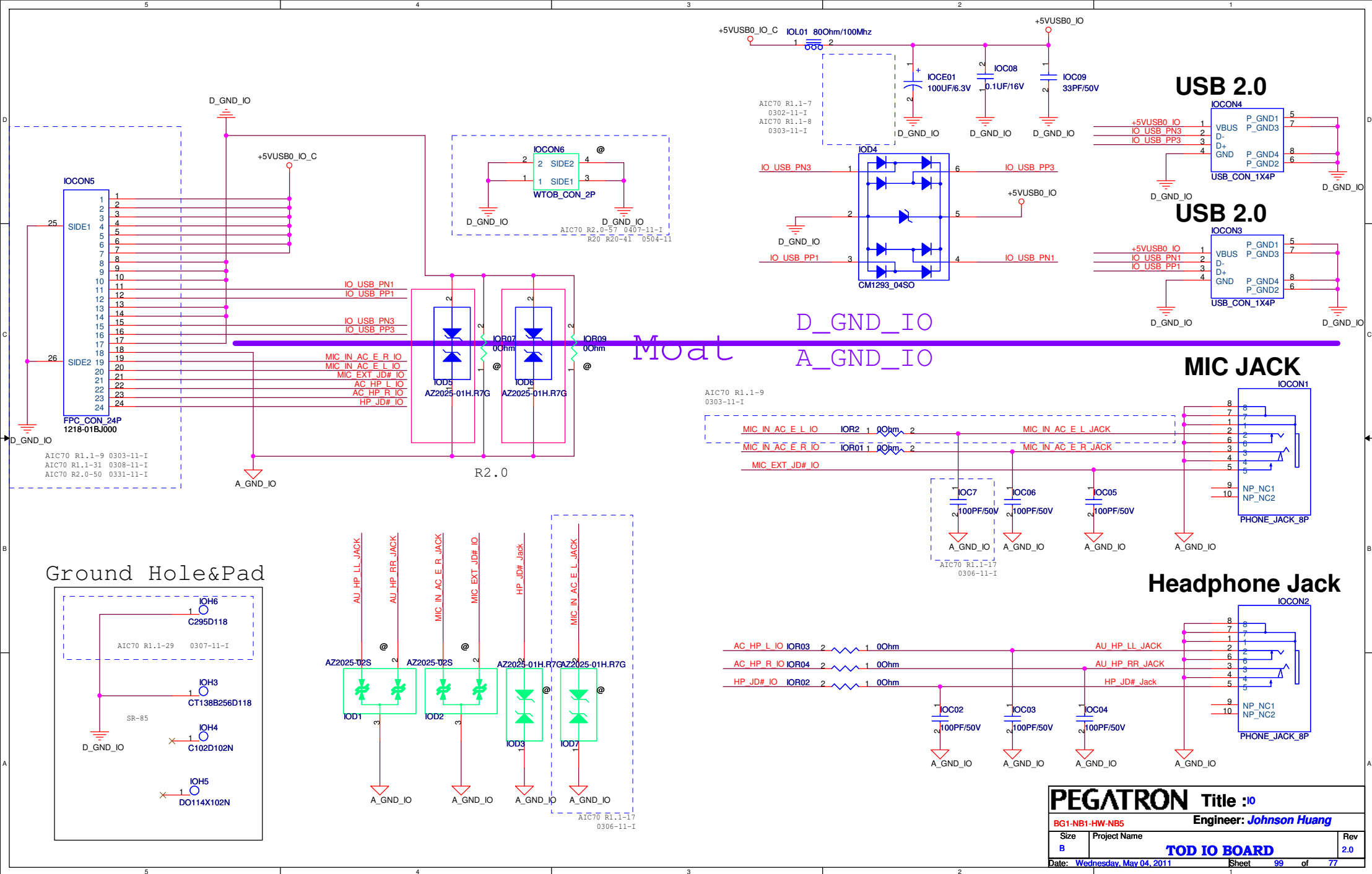


LID Switch



AIC70 R2.0-48 0330-11-I
AIC70 R2.0-67 0421-11-I

PEGATRON		Title : A03 TP	
<OrgName>		Engineer: Johnson Huang	
Size B	Project Name AIH70		Rev 1.0
Date: Thursday, April 21, 2011		Sheet 98 of 99	



PEGATRON Title :IO		
BG1-NB1-HW-NB5		
Engineer: Johnson Huang		
Size	Project Name	Rev
B	TOD IO BOARD	2.0
Date: Wednesday, May 04, 2011	Sheet 99	of 77